

Chapter 5 - System Design using Standard Converters

The use of standard power modules has made system design much easier. However, the designer must still understand how the power converter interacts with external circuitry such as input filters and diagnostic circuitry. Paralleling of power converters is now becoming important due to increased redundancy requirements and the system designer must understand how this is achieved. This chapter sets out a methodology whereby a system designer can implement the power solution in the system.

5.1 Introduction

With the present availability of standard power solutions, the job of the power system designer has become significantly easier. There is no longer a need for detailed attention to the circuit operation and reliability of the internal implementation of power converters because the proven standard designs result in a robust and reliable power system with minimal technical risk. The power system designer is thus freed up to concentrate on the system aspects of the design. It is assumed that the power architecture has been selected based upon the principles outlined in Chapter 3 and appropriate power converters have been specified based upon the information presented in Chapters 1, 2 and 4.

We now turn to the aspects of the system design that will insure the success of the product. These areas of design will tend to focus on the interfaces between the power converter(s) and the remainder of the system - input circuits, output distribution considerations, controls, diagnostics and paralleling. Each of these areas will be explored in some detail with the intent of highlighting the aspects that will have the largest influence on the performance of the overall system. Hopefully the priorities and design tips presented here will help to demystify the process of designing a reliable and cost-effective high performance power system.

5.2 Input Design Considerations

Certainly one vital interface to a power converter is the connection to the input power! Compared to the output connection, the input interface tends to be much more standardized and predictable because the converter is usually operating from either the AC power mains or from some kind of Telecom DC bus. These sources are controlled by many standards and industry conventions so that the input circuitry of equipment power systems is often very similar. The main system design issues will be safety (conductor sizing

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and fusing) and immunity from input power transients. We will discuss these considerations for both AC input and DC input power converters. We will also be addressing some other system requirements including reflected ripple, input voltage operating range, the need for and selection of input capacitors, hot plugging and primary-side control functions.

AC Input Converters - Artesyn's line of standard AC/DC converters are designed to accommodate worldwide AC mains standards, and will provide reliable performance when properly installed in the end use equipment. This installation only needs attention to the most normal considerations, such as safety and immunity from powerline transients.

The most important safety related design items are grounding, fusing, and proper conductor selection. An AC input power converter will have a chassis safety ground connection included on the input connector. It is imperative, for purposes of safety, that this pin is connected to the "green wire" ground of the AC power mains. This requirement is in addition to the chassis bonding requirements that may apply. Most AC/DC converters will contain either a fuse or circuit breaker internal to the unit which is rated so that it will protect the converter itself from creating a fire hazard in the event of an internal fault. Note that this internal current limiting will not protect the wiring that connects the converter to the AC powerline. In the event of a short circuit between the input conductors, this fuse or circuit breaker will not activate, and the current in the conductors will be limited only by the line impedance or an external fusing device. This external fuse or circuit breaker is located at the front end of the equipment box, often in the area of the input EMI filter. The sizing of the

AC conductors to the power converter and the trip rating of the fuse or circuit breaker must be coordinated so that the circuit will open before the conductors reach a dangerous temperature. Note that, in general, these conductors must support the current for more than one converter. Figure 5.1 summarizes the safety-related issues of connecting the input power to an AC/DC converter. It depicts input wiring for a 208/240V line-to-line application. The input connection will be similar for a line-to-neutral 100/120V connection, except that no fuse will be required in the neutral conductor. Many, if not most, high quality AC/DC converters now include an automatic input voltage ranging function as part of the PFC circuitry, allowing for operation from below 100V to over 250V. This simplifies the power system design because jumpers or different connection points to the converter are no longer required to configure it for either line-to-neutral or line-to-line applications.

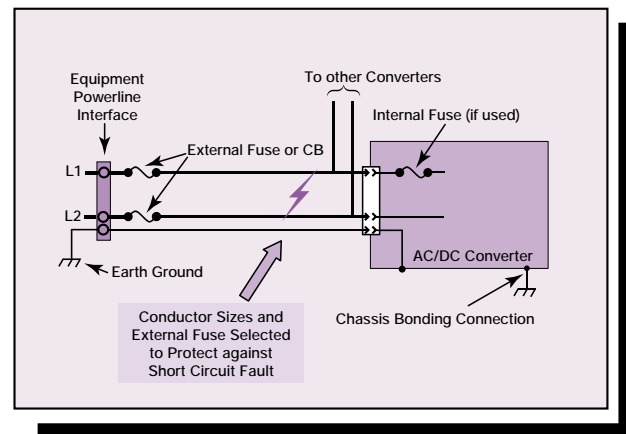


Figure 5.1 - Safety Consideration of AC Input Connection

Keep in mind that the AC/DC converter will have an input current surge each time that the AC power is applied. This current will be higher than the normal operating current, and is caused by the need to charge up the

capacitors on the output of the off-line rectifier circuit. The magnitude and duration of this surge should be specified by the converter manufacturer. With well-designed converters, the current will be manageable. Make sure that whatever circuitry is located in front of the power converter can handle this surge current. Pay special attention to the current vs. time profile of the fuse or circuit breaker to insure that you will not experience any nuisance tripping when the AC power is simultaneously applied to all the power converters.

In general, the system will require some sort of EMI filter near its input, the primary function of which is to reduce the conducted emissions from the equipment that are imposed on the powerline. The need for and selection of the EMI filter will be covered in more detail in Chapter 9.

Many systems are designed to comply with the so-called Electric Fast Transient (EFT) or Burst Immunity requirement as defined in specification EN61000-4-4. This requirement attempts to simulate the type of impulses that can result from contactors, relays and switches being activated elsewhere in the system. The bounce from such contacts opening and closing can create high frequency but relatively low energy voltage transients on the AC input lines. Meeting EFT is a system-level requirement, but some AC/DC converters, including Artesyn's, will meet this specification as a stand-alone device. The addition of the system EMI filter and other components in the system's AC Front-End generally makes adherence to this requirement even easier. There are several versions of the EFT with varying severity for different system environments, but the values most commonly encountered by Telecom and Datacom power converters, level 3 and level 4, are shown in Figure 5.2. Note that the values shown in the diagram are the

open circuit output from the test signal generator and that when it is coupled through capacitors to the low input impedance of the actual powerline, the voltage values will be substantially reduced. If you select high quality AC/DC converters that are designed to meet the EFT requirement and pay attention to normal AC distribution design practices you should not have a problem with the EFT requirements.

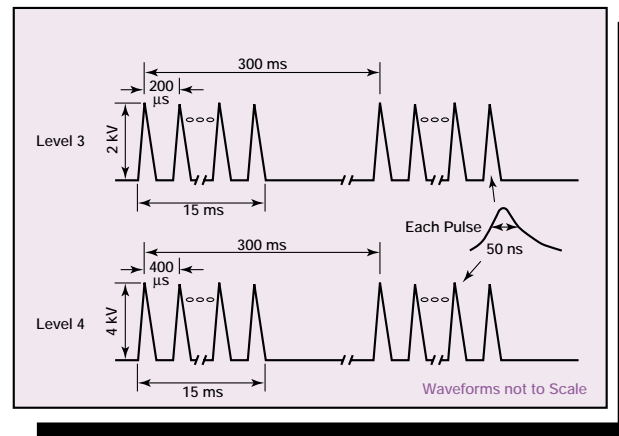


Figure 5.2 - Electrical Fast Transient Immunity

The least complex input circuit design will occur when using Artesyn's AFE family of standard Front-End products, shown in Figure 5.3. These AC/DC converters are supported by a series of standard power shelves that perform several functions while relieving the power system designer of the corresponding design tasks. The power shelf contains circuit breakers and an input filter to support the Front-End converters so that these devices do not need to be included elsewhere in the system. (Note that the system may still require another circuit breaker and/or EMI filter if there are loads not powered by the Front-End converters) This system will also support "hot plugging" of the converters so that concurrent maintenance can be provided for high-availability systems with redundant AC/DC converters. It

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also provides a self-contained low-powered source of 12V and convenient system level diagnostic and control signals to and from the AC/DC converters to simplify the system power interface and monitoring.



Figure 5.3 - Artesyn AFE Standard Front-Ends with Power Shelf

DC Input Converters - DPA systems have only become popular for other than Telecom usage in recent years. As a consequence, many power system designers are not as familiar with the proper configuration of input circuits for DC/DC converters as they are with the AC interface to off-line AC/DC converters. It is a very different environment, since there is either a battery bank or an AC/DC converter in front of the DC/DC rather than an AC powerline. Each system will be slightly different, and the resulting DC source will not be as standardized as the power utility. Nevertheless, there are some general principles that will lead to a successful input circuit design. As we discuss them below, it will be seen that they are sensible and easily understood. For purposes of simplicity, the input design issues will be illustrated with a single DC/DC converter operating from a 48V Telecom bus. As will be seen later, it is often possible to share common input circuits between several converters, making the overall design much less complex and more cost-effective. Design for alternate input voltage busses, such as 24 or 60V nominal, will be very similar in concept.

The input terminals of the DC/DC converter are connected directly to the intermediate voltage source. Artesyn's converter modules operate over a wide input voltage range making them very robust and immune from fluctuations in input voltage. For example, DC/DC converters intended for the 48V Telecom bus can have an operating range from 36V to 75V, and the input voltage will almost always stay within this broad range. But be aware of what could happen if the input voltage exceeds either extreme. If the input voltage exceeds the maximum rated input voltage, the converter could be damaged from excess voltage stress. If the input voltage goes too low the input current will increase and possible excess current stresses could occur. For these reasons, many converters have a built-in mechanism that monitors the input voltage. These features are referred to as undervoltage lockout (UVLO) and input overvoltage protection.

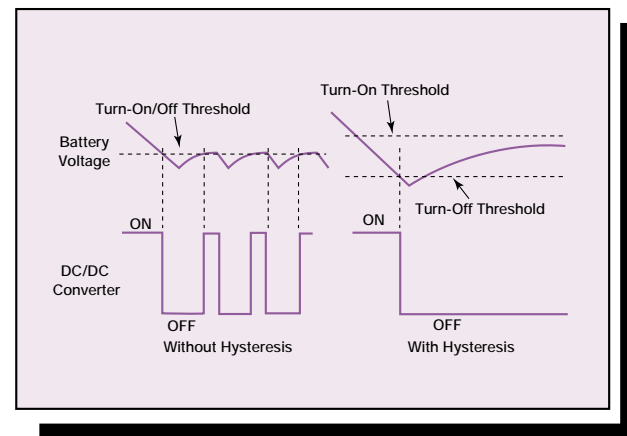


Figure 5.4 - Value of Hysteresis in UVLO Circuit

Using converters that incorporate the above features can simplify your system design. The input overvoltage protection eliminates the need for expensive and difficult to design overvoltage detection and clamping circuits on

the input. UVLO, in addition to preventing damage to the converter itself in the event of a low input voltage situation, has some system-level benefits. One major benefit is that it helps prevent deep discharge of batteries supplying the DC input when the DC input rail is down. Deep discharge will eventually damage a battery so UVLO helps it maintain maximum operating lifetime. The UVLO circuit will include hysteresis, so that the converter turn-on voltage level is higher than the turn-off level. Without this feature, when the converter turns off due to battery discharge on the intermediate bus, the battery load will decrease and the battery output voltage will slightly rise, turning the converter back on again. This can result in a low frequency oscillation, with the converters in the system constantly turning on and off, as shown in Figure 5.4. The hysteresis solves this problem because the increase in battery voltage at converter turn-off will not be enough to activate the higher turn-on input voltage setting. The UVLO will also protect the system backup batteries from excessive discharge, turning the converters off when the battery voltage reaches a dangerously low value. Some Artesyn converters, such as the SXA10 series, allow for easy user programming of the UVLO levels by means of a single external resistor.

Most DC/DC converters offer a provision for remote turn-on and turn-off. This feature is not needed if you want the converter to power up automatically when the Front-End converter is activated. With an "active high" converter, there is no need to make any external connections to have the converter power up automatically. Some converters are designed with or have an optional "active low" arrangement. If this is the case, there is a provision for automatic activation, normally by just jumpering the remote on/off pin to another pin on the converter (usually the input return). This allows for an essentially zero cost method of

bypassing the remote on/off feature and switching the DC/DC converter on and off with the remainder of the system. There are situations, however, in which separate on/off control of a DC/DC converter is desirable:

- Need for **Sequencing** application or removal of individual voltage levels
- Powering down sections of the load circuitry when not needed
- Protecting DC/DC without UVLO from low input voltages
- Putting DC/DC into a low power "standby" state

The fourth item above may require additional explanation. In the case of many of the better DC/DC converters, if it is inhibited by the remote on/off, most of the internal circuitry is completely powered down. This results in significantly less converter power consumption than running the converter with zero load current, and can be a significant advantage in portable products or other equipment that places a high value on overall efficiency. This inhibited or "sleep mode" power should be specified in the converter data sheet.

The converter data sheet should be consulted to determine the proper interface for driving the remote on/off pin. In many cases, it is set up with an internal resistor for use with a simple open collector pull-up. This arrangement makes for very simple control from either a discrete external transistor, an open collector TTL chip or opto-isolator. The on/off control signal return is usually the negative input voltage terminal of the converter. The converter data sheet should specify the turn-on and turn-off voltage levels as well as the minimum current sinking capability of the driving device, which is usually

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very modest ($<200\mu\text{A}$) so that a small-signal device can be used. It is also possible to use a "totem pole" active-high TTL IC with some converters, but not all of them, since the internal pull-up voltage of some converters is higher than the TTL voltage limit. Also be cautious of using active-high driver circuits with converters that have an adjustable UVLO function. In this case, a diode must be added between the driver and the converter to prevent the active-high driver circuitry from influencing the UVLO levels. If a relay (or mechanical switch) is used for control of the remote on/off function, be aware that the contact bounce may result in multiple converter on/off activations and a DC output waveform that isn't a smooth ramp.

Almost all DC/DC converters implement their on/off control function on the input side of the converter, while the system power control circuitry often resides on the output side of the converter. This presents no particular problem when using non-isolated converters since the input side and the output side share a common ground. In the more common case of isolated converters, however, the input return is kept separated from the output return. In order to maintain this isolation, some form of isolated interface must be used between a secondary-referenced control system and the converter primary side remote on/off pin. Isolation is sometimes done by means of a signal transformer or relay, but by far the most common method is to use an opto-isolator.

In noisy environments, it is recommended to put a low value ($\sim 100\text{pF}$) capacitor across the remote on/off control pins. This is a good precaution, in fact, for all converters as it provides additional robustness at a very modest cost. Figure 5.5 shows the typical remote on/off interfaces of many DC/DC converters. This discussion

has been general in nature, so make sure to check the latest data sheet and application notes of the converter you are using to determine the specific requirements for interfacing to the remote on/off pin.

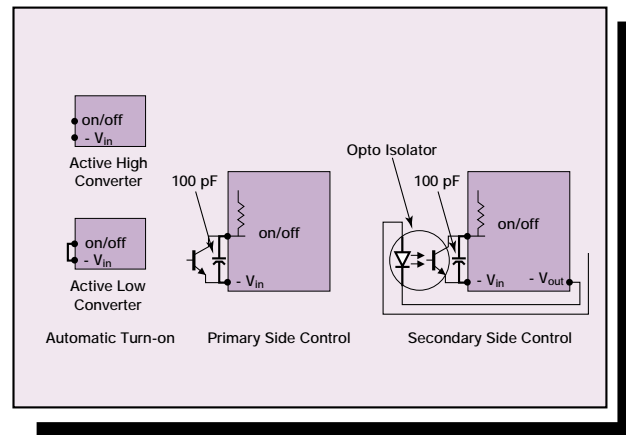


Figure 5.5 - Typical Remote On/Off Connection

The inclusion of an **input capacitor** across the input power terminals of a DC/DC converter is almost always a wise decision. This addition is often recommended in the applications literature by the DC/DC manufacturer, especially for higher power models, and can serve several functions:

- Reduces the converter input ripple current seen by the system
- Reduces the source impedance to the converter
- Reduces conducted EMI levels

Because of the stress levels on this part, electrolytic capacitors are not recommended except for high power converters. The best choice for converters of 50W or less is usually a film or ceramic capacitor in the range of 4 to 10 μF with a 100V rating (for a 48V Telecom environment). Consult the applications literature for the

converter you are using for more specific recommendations. The SimScope tool, which is available on Artesyn's website, can assist with making the proper selection of the input capacitor. The SimScope simulation will show how the input ripple current to the converter varies as a function of the input capacitor value, its equivalent series resistance (ESR) and equivalent series inductance (ESL). We will see later how this capacitor can also help with making the converter more tolerant of faults occurring elsewhere in the system.

The two primary **safety** related design issues on the input side of a DC/DC converter are the safety rating of the input source and fusing of the converter. Most DC/DC converters will be designed with **basic insulation** and are intended for usage only with an input source (intermediate bus voltage) that is either

- Safety Extra Low Voltage (SELV) Circuit
- Telecommunications Network Voltage (TNV)

and is isolated from the power mains by **reinforced insulation**. Most Telecom central office installations or Front-End AC/DC converters will provide for this requirement. More information relative to the required safety standards in different equipment types and markets is contained in Chapter 10.

Fusing is an important design consideration for DPA systems. DC/DC converter modules will, in general, not contain an internal fuse. The fuse is best located externally for several reasons:

- User accessibility
- Replacement without removing converter

- Sharing a single fuse between several converters

The fuse actually serves two purposes. In the event of a short circuit fault on the input side of the DC/DC converter, the fuse will prevent excessive fault current from flowing in the PCB and prevent overheating and charring of circuit traces. The fuse will also disconnect the failed converter group from the remainder of the system. Without a fuse, the intermediate voltage bus could be overloaded and the resultant voltage reduction could force other converters in unrelated parts of the system to shut down. With a properly sized fuse in place, the remainder of the system will continue running.

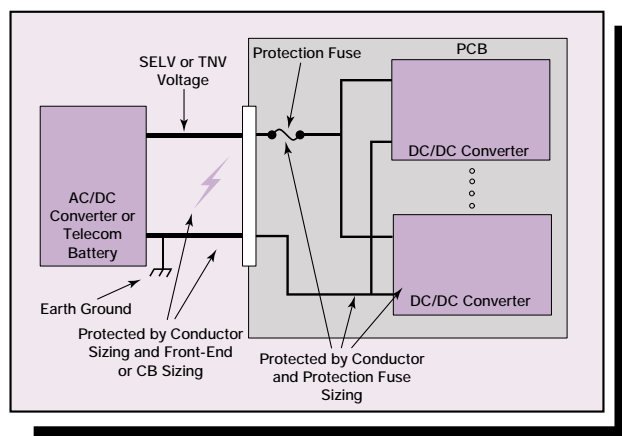


Figure 5.6 - Safety Considerations of DC Input Connection

If the DC/DC converter input is an earthed circuit, the fuse must be located in the unearthed side of the input, as shown in Figure 5.6. This is done so that the circuit will remain earthed in the event that the fuse opens. If the DC/DC converter is unearthed, the fuse could be located in either leg of the input circuit. The current rating of the fuse will, of course, depend upon the power level of the DC/DC converter. For 48V nominal input systems, the most commonly recommended current rating will fall in the range of 0.5 to 5A. A 200V anti-

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surge or slow-blow high rupture capacity (HRC) fuse is normally used. It is important to consult the data sheets and application notes for the DC/DC converter you are using to obtain the specific fuse recommendation. Artesyn supplies this information for all of its products. The failure rate of the fuse can be higher than that of many other components. In order to maintain your system reliability goals, it is important to use high quality fuses and to consider sharing fuses between converters in order to minimize the number used.

The most common high frequency input transient requirement for DC/DC converters is the same EN61000-4-4 **Electric Fast Transient (EFT)** specification as described in Figure 5.2. In this case, the transients are applied to the intermediate bus voltage. The DC/DC converter data sheet should state the level of immunity that is designed into the converter. There is no need for specialized power system design in this regard, although usage of an input capacitor on the converter will create extra margin for transients as well as providing the other advantages described elsewhere.

The most severe transient condition in distributed power systems occurs during fault conditions in large systems with multiple fault groups protected with fuses or circuit breakers. The transients are due to the undervoltage condition during the time before the fault clears and the overvoltage condition caused by the system distribution inductance after the fuse or circuit breaker opens. These transients will contain substantially more energy than the EFT. Each system will be different and require its own analysis to obtain quantitative data. We will present here a generalized discussion so that the principles involved can be understood. We will also discuss the most commonly used techniques for minimizing the surges

and for keeping them from disrupting the operation of the remainder of the system. For the next higher level of detail on this type of analysis, the content of the European Telecommunications Standards Institute (ETSI) technical report ETR 283 "Transient Voltages at Interface A on Telecommunications Direct Current Power Distributions" is highly recommended.

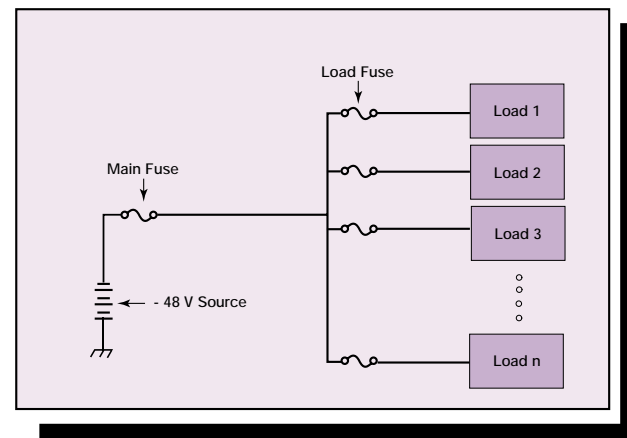


Figure 5.7 - System Configuration for Fault Transient Analysis

Figure 5.7 shows a generalized representation of a DPA system containing multiple loads and fault groups, all of which are powered by a common -48V nominal telecom bus with fuses or circuit breakers in the unearthed negative conductors. A single equipment enclosure is shown, which could be one cabinet in a telecom system powered from the central office battery or a single enclosure datacom system powered by an AC/DC converter with or without battery backup. Note that in the case of a true telecom system, several enclosures may be connected to the same 48V battery source. In that case, the complete fault transient analysis will need to include the entire interconnected system. Fortunately for the purposes of analysis, the most severe transient interactions will occur with the load groups physically closest to the fault location - i.e. within the same

enclosure. For that reason, only a single enclosure will be used for this general discussion. Each load group will be protected by a fuse or circuit breaker. We will use the term "fuse" here to refer to either choice of circuit protection. There will also be a higher capacity fuse to protect the larger main distribution conductor. There will be corresponding conductors for the return circuit, but only the negative ungrounded conductors are shown here for purposes of simplicity in the diagrams. The intent of the fault transient design is to prevent disruption to other load functions when a fault to earth occurs in one load function.

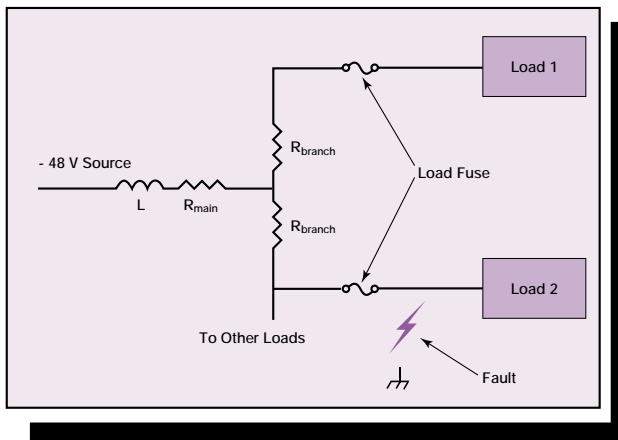


Figure 5.8 - Fault Circuit Assumption

The circuit we will assume for purposes of this discussion is shown in Figure 5.8. It shows two physically adjacent load groups of the generalized system shown in Figure 5.7. We will assume a fault to earth occurs in Load 2 as shown and evaluate its effect on the input voltage to Load 1. L represents the total inductance of the distribution conductors that are shared by loads 1 and 2. R_{main} represents the total resistance of the distribution conductors before the branching between circuits occurs. R_{branch} is the resistance of the feeder distribution to each load group. All of these component

values also include the return conductors even though they are not shown in the diagram.

At the initiation of the fault, a large fault current will flow through the fuse for Load 2. This current will be limited only by the total resistance in the circuit, R_{total} , and the R/L time constant. R_{total} includes:

- R_{main}
- R_{branch}
- Resistance of Fuse
- Resistance of Fault
- Internal Resistance of the -48V source

The fuse will not open until the current through it exceeds its rating for a period of time determined by its construction characteristics. Thus, the fault is not cleared instantly, and there is a definite period of time during which the intermediate bus is shorted to earth. This situation is shown in Figure 5.9. During this time interval, the fault current will rise exponentially as shown in the figure according to the expression:

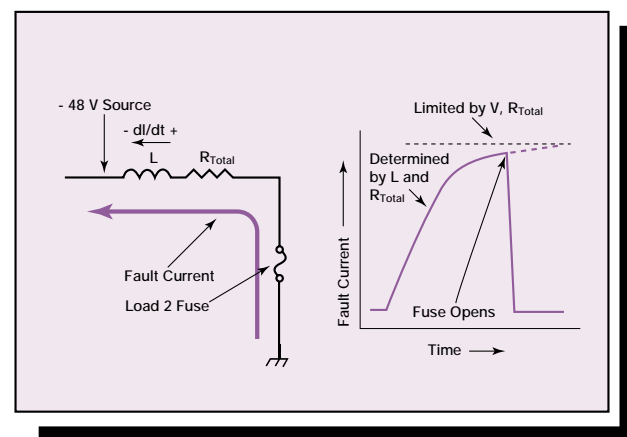


Figure 5.9 - Fault Current

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$$\text{Fault Current} = \frac{V}{R_{\text{Total}}} \times \left[1 - e^{-\frac{R_{\text{Total}}}{L} t} \right]$$

Equation 1

where: V = Source Voltage
 t = time

This exponential rise will continue toward the steady state fault current determined by the source voltage and R_{Total} until the current is interrupted by the fuse. At this point, the fault current falls to zero. Note that battery voltage sources can have a very low source impedance, and the fault current can be well in excess of the fuse ratings. Fault current capability in excess of 1kA can be possible in Telecom systems. During the time the fault current is flowing, energy is being stored in the distribution inductance, L , and reaches a maximum value of:

$$\text{Stored Energy} = \frac{LI^2}{2}$$

Equation 2

where I = maximum fault current prior to fuse opening

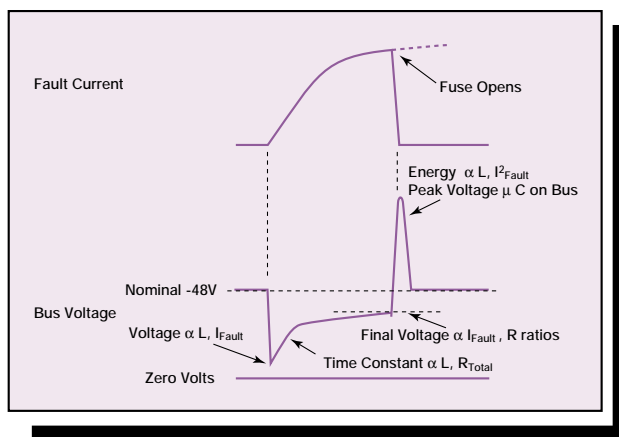


Figure 5.10 - Generalized Bus Voltage Waveform During Fault

The fault current will affect the intermediate bus voltage in the remainder of the system as shown in Figure 5.10. The bus voltage shown there is the voltage at the input to Load 1. There will be an initial decrease in the bus voltage due to the $L \, di/dt$ voltage drop across the distribution inductance. This initial inductive drop can reduce the instantaneous bus voltage to as little as zero volts. As the fault current builds to its maximum the inductive drop becomes less and the bus voltage will reach a "steady state" value determined by the ratios of the distribution resistances unless the opening of the fuse interrupts it first. When the fuse opens, the energy stored in the distribution inductance is released into the system. The di/dt of the rapidly falling fault current is in the direction to make the bus voltage at Load 1 more negative (increased bus voltage). This will result in an overshoot voltage transient on the intermediate bus with energy content roughly equivalent to the stored energy determined in Equation 2.

Even a brief examination of Figure 5.10 reveals that there are two possible problems in terms of maintaining operation of the DC/DC converters powering Load 1. First, there is a rather severe drop in the bus voltage during the time that the fault current is flowing, especially at the initiation of the fault. Secondly, if the bus voltage overshoot that occurs when the fault clears is high enough, it could damage the converter due to excessive input voltage stress. While these are both reasonable concerns, we will see that they can be easily managed with proper power system design. The techniques we will discuss fall into three categories:

- Minimizing energy stored during the fault
- Maintaining operation through the initial undervoltage condition

- Handling the stored energy after the fault clears

First, let's see how we can minimize the stored energy. From Equation 2 we know that reducing distribution inductance and/or the fault current will have positive benefits. There are several design parameters that can help in reducing inductance:

- Use physically large cross-section conductors
- Keep conductors as short as possible
- Run bus and return conductors next to each other
- Use low permeability insulation

Given a fixed source voltage, the "steady state" fault current is determined by the total resistance in the fault circuit. That being the case, additional resistance in the distribution network could actually be helpful. This approach is referred to as "**high Ohmic distribution**". As we will see shortly, the location of this resistance is critical to other aspects of the fault tolerance design. Since this approach slightly reduces the efficiency of the power system and complicates the design, it has not been universally adopted. Note from Equation 5 and Figure 5.9 that the fault current is not constant, but rather rises exponentially from zero towards its "steady state" value. This means that the maximum fault current will be a function of the time that it takes for the fuse to open. Faster acting fuses will minimize the fault current and consequently the stored energy. Unlike the resistive approach, there are no negative tradeoffs with the use of faster acting fuses or circuit breakers. In general, fuses will be faster with opening times in the range of 1 to 10mS compared to 4 to 15mS for circuit breakers. In summary, then, reducing distribution inductance and the fuse response time and possibly increasing the

distribution resistance will all help reduce the energy stored in the distribution system due to a fault condition.

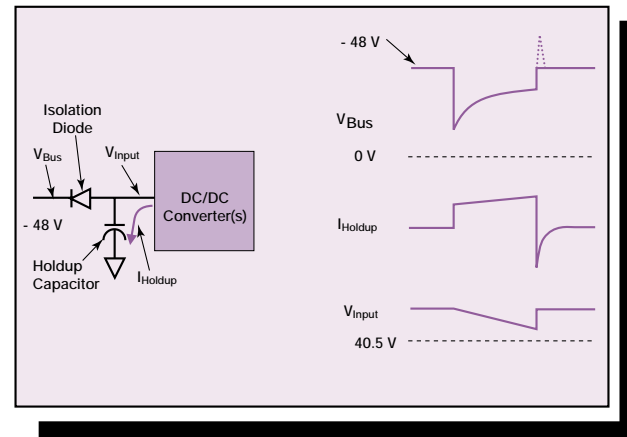


Figure 5.11 - Hold-up Circuit

The lower operational steady-state limit for the standard Telecom bus is 40.5 Volts. The better DC/DC converters are designed to operate down to perhaps 36 Volts. The voltage waveform in Figure 5.10 goes below these values for at least a portion of the duration of the fault current. Operation of Load 1 during this time is assured by means of a **holdup** circuit as shown in Figure 5.11. The circuit consists of only two components, a diode and a capacitor. The diode becomes reverse biased during the undervoltage portion of the fault and isolates Load 1 from the intermediate voltage bus during this time. The capacitor is used as a source of energy for the DC/DC converter(s) that power Load 1 until the fault clears or the bus voltage rises to an acceptable level. The size of the capacitor is a function of the desired **holdup time** and the power requirement of the converter(s). The capacitor is selected so that it will not discharge below the 40.5V Telecom lower voltage limit during the expected hold-up time. Lower inductance and faster clearing fault management circuits will require smaller holdup times. For systems utilizing a positive voltage input, the diode

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direction would be reversed.

The low Ohmic resistance approach alluded to earlier can also be used to minimize the required holdup time. In general, the "steady state" voltage during the fault time will be a function of the voltage divider determined by:

$$\text{Steady State Fault Voltage} \propto \frac{R_{\text{branch}}}{R_{\text{main}} + R_{\text{branch}}}$$

Equation 3

Thus, by sizing the conductors in the final stages of the distribution to achieve higher resistances there (i.e. $R_{\text{branch}} > R_{\text{main}}$), the bus voltage can be made higher during the final stages of the fault and the holdup time minimized. With proper design, this final bus voltage can even be high enough to allow operation of the DC/DC converters without assistance from the holdup capacitor, minimizing the size of the capacitor required. Please note that this analysis is rather simplified and that each branch will actually have different values of distribution resistance. These varying resistance values and the relative locations of the possible faults and other loads will need to be considered. Some typical bus voltage waveforms and relative holdup times that can be achieved by these techniques are shown in Figure 5.12.

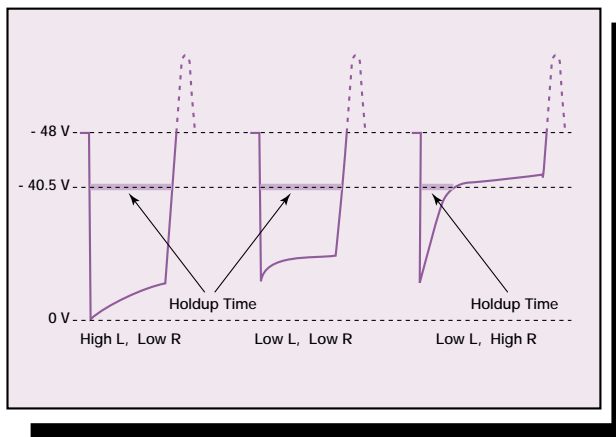


Figure 5.12 - Undervoltage Bus Waveforms vs. L and R Values

For the low inductance, high Ohmic option shown in the rightmost waveform, the fault clearing time is longer due to the reduced fault current. But note that the bus voltage recovers much more quickly to the lower Telecom voltage limit so that the required holdup time is reduced. This can be a good design approach. In addition to reducing the holdup time and associated holdup capacitor values, it will more readily allow the usage of circuit breakers instead of fuses, since the fault clearing time is no longer as critical. Time constants in the range of 10 μ S to 1mS are achievable using this technique.

As an example of how the holdup capacitor would be selected, consider a system where Load 1 consumed 20W from the bus and the typical holdup time requirement based on the distribution system characteristics was determined to be 100 μ S. The DC/DC converter will operate down to 36V. First, calculate the average current requirement of the load. The current at the nominal 48V bus voltage would be 20W/48V = 0.42A. But the current draw will increase as the holdup capacitor discharges since it is a constant power load. At the 36V lower Telecom limit, the current will be 20W/36V = 0.56A. Therefore, the average current requirement will be about 0.49A. The allowable voltage drop is 48V - 36V = 12V. From the relationship:

$$C = I \frac{dt}{dV}$$

Equation 4

we determine that $C = (0.49)(100 \times 10^{-6})/12 = 4\mu\text{F}$.

This capacitance does not need to be composed totally of dedicated holdup capacitors. Any input capacitors that have been used at the input of the DC/DC

converter(s) on the board will contribute as well as capacitors in input filters. Remember that input capacitance also has other benefits such as EMC control and reduction of input ripple. A more convenient and accurate method of calculating the required holdup capacitor value is to use the automated calculator supplied by Artesyn as part of their on-line Virtual Power Lab. You enter the required holdup time, the beginning and ending voltage values and the load power and the calculator will return the required capacitor value. There is also a similar calculator that will provide the holdup time for a given value of capacitor.

We have seen how to minimize the energy stored in the fault and how to design the remaining loads so that their operation is not disrupted. The remaining issue is how to handle the voltage overshoot that occurs at the time the fault clears. Remember first of all that the energy content of this transient and consequently its voltage level will be determined by the stored fault energy. So reducing the stored energy as discussed above will also pay big dividends in reducing the overvoltage transient.

Assuming that the total stored energy has been minimized, we have two choices of how to handle it at the time of fuse clearing. It can either be dissipated or stored for later use. One possible way to dissipate some of it is to use special fuses or circuit breakers that are designed to arc when opening and that dissipate energy in the arc. These devices are relatively new and not yet in widespread usage, but could show promise. The more commonly used dissipative technique is to use high power Zener type semiconductors across the intermediate bus. They must be selected and tolerated so that the lowest activation voltage is above the worst case Telecom abnormal service voltage - 60V. They of

course add complexity and cost to the power system design as well.

Perhaps the most widely used technique for handling the overvoltage transient is to use it to charge capacitance connected across the intermediate voltage bus. This will reduce the amplitude of the voltage spike and make the energy available for later use by the load converters. Assuming the transient energy is equal to the stored fault energy, we can use the energy balance equation to determine the required capacitance for any desired maximum voltage level:

$$\text{Stored Energy} = \frac{1}{2} L I^2 = \frac{1}{2} C V^2$$

Equation 5

Solving for C:

$$C = \frac{L I^2}{V^2}$$

Equation 6

where I = maximum fault current

V = desired maximum transient voltage

L = distribution inductance

Figure 5.13 shows how the addition of capacitance will make the overvoltage transient much more tolerable. This approach tends to be very efficient since all of the energy transferred to the capacitance can be used to power the load. The required capacitance is easily managed in most systems, as the holdup capacitors at the loads will also contribute. Enough capacitance should be used so that the maximum transient voltage is less than the maximum rated voltage of the DC/DC

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converters or other components attached to the front end - often in the range of 75 to 80V.

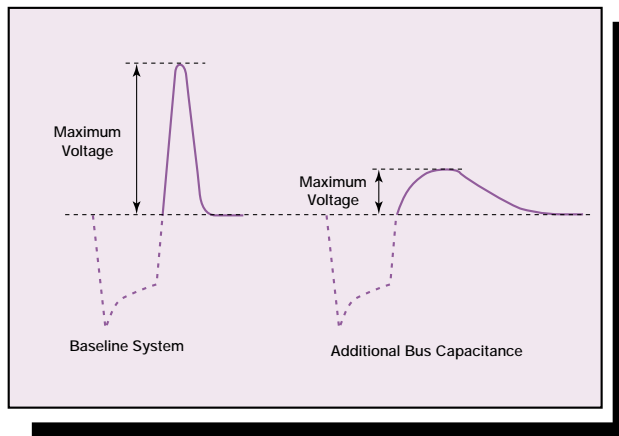


Figure 5.13 - Reduction of Transient Voltage with Bus Capacitance

The relevant standard for the power interface to Telecom equipment is ETS300 132-2. The reader is directed to this document for the latest design requirements and test waveforms. As mentioned earlier, ETSI ETR 283 is a very valuable reference for analysis of techniques for minimizing transient voltages and maximizing the system immunity from them.

One of the input circuit design considerations for DC/DC converters is the amount of high frequency (converter operating frequency and higher) current content on the intermediate voltage bus. These currents will contribute to the overall conducted emissions performance of the system. **EMI design** relates to the system as a whole rather than to a specific converter and EMI solutions are typically provided at a system level or sub-assembly level rather than having a filter on each DC/DC converter. EMI will be covered in more detail in Chapter 9, but we will make some general comments here based on the simplifying assumption that we are focusing the conducted emission solution on only one converter.

Each DC/DC converter design is different and there is no rule-of-thumb for conducted emission performance that can be applied to all of them. The EMI performance will generally be better for lower power converters than higher power ones and the products from the higher quality suppliers such as Artesyn will generally contain more attention to the details of EMI design, including some internal filtering components. Meeting the EN55022 class A requirement may only require the addition of a single input capacitor for low power converters. Meeting the more stringent class B limits will generally require using a single section external filter for low power converters and perhaps a more complex filter geometry for high power converters. Some advanced products, such as Artesyn's SXA10 series will require no external components to meet class A, and only a small input capacitor to meet class B. Make sure to consult the applicable data sheets and applications information for the latest information on the converter family that you are considering. If the filtering is done at a converter or PCB level, the input currents are low and the required filter components will be physically small, inexpensive, and suitable for automated assembly. Figure 5.14 shows the generalized filter configurations most commonly used with on-board DC/DC converters. If more than one converter is used on a single PCB, a single shared filter at the board level usually is used for filtering with a significant reduction in total component count.

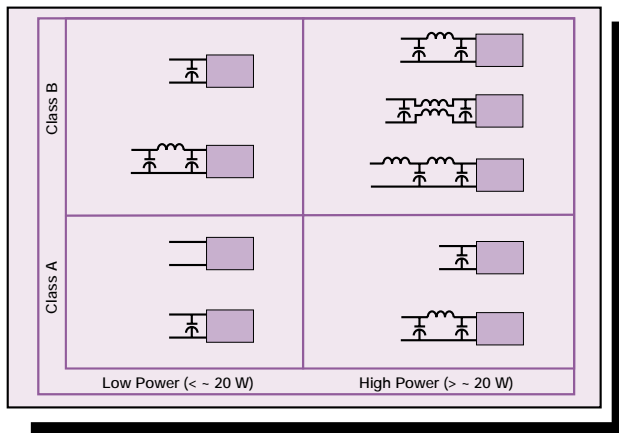


Figure 5.14 - Generalized DC/DC Converter Conducted Emissions Filter Configurations

Another significant factor in controlling the EMI environment on the input side is the **circuit board layout**. The high current switching circuitry on the primary side of the converter is referenced to the input source voltage or its return. Keeping the converter primary circuits as close as possible to one or more sizable conductive planes at these potentials will help keep the high frequency fields contained to as small an area as possible and consequently minimize radiated EMC and interaction with other components. The ideal situation is a PCB with two or more layers so that dedicated planes can be used in the area of the converter for the input source voltage and its return. These planes can then be extended over the entire input side of the converter as shown in Figure 5.15a. A similar arrangement is used for the secondary output and its return. In the case of a single layer board, a split plane arrangement, such as that shown in Figure 5.15b can be used. More specific layout information, including how to handle multiple output converters, can be found in the appropriate application notes for the converter in question. Note that the primary and secondary conductors of these planes **must** be separated by the

minimum required spacing to insure meeting the creepage and clearance requirements of the applicable safety standard. Additional information on the safety related aspects of the PCB board layout can be found in Chapter 10.

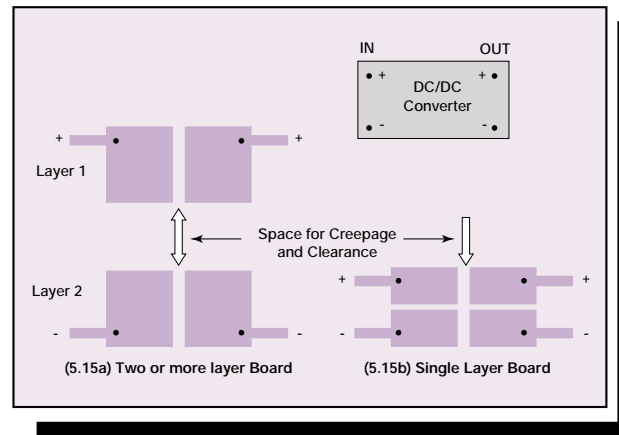


Figure 5.15 - General PCB Layout for Minimizing Radiated EMI

High availability is becoming a much more important system requirement, and has resulted in the need for "live insertion" or "hot plugging" of circuit boards containing DC/DC converters. These boards typically have relatively large values of capacitance across the intermediate bus input, comprised of capacitors for converter inputs, EMI filter, and holdup. If the circuit board is plugged into the bus of an operational system with these capacitors in a discharged condition, an inrush current transient will occur as these capacitors are charged from the low impedance intermediate voltage bus. This inrush current can create several undesirable conditions:

- High current stress and arcing on connector pins
- High stresses on input components
- Temporary voltage dip on the intermediate bus

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There are several design techniques that can be used to control the inrush current. We will describe three of them here. The use of one of these design approaches will allow hot plugging of circuit boards without stressing either the card being inserted or the remainder of the system.

The simplest technique is the so-called "long pin" approach. Some connector systems have the provision for making some of the pins different lengths so that some of them will make contact before others when the connectors are mated. If two long pins are used as shown in Figure 5.16a, a resistor can be inserted in series with the intermediate voltage bus when the circuit board is inserted. This resistor is then shorted out after the other pins make contact. The series resistor will limit the charge current and allow the input capacitance to charge up in a more gradual fashion. This approach has the advantages of simplicity and low cost. On the down side, it requires the utilization of a specialized connector system. It will also have no effect on any turn-on surges that occur when the system is powered up with the circuit board already plugged in.

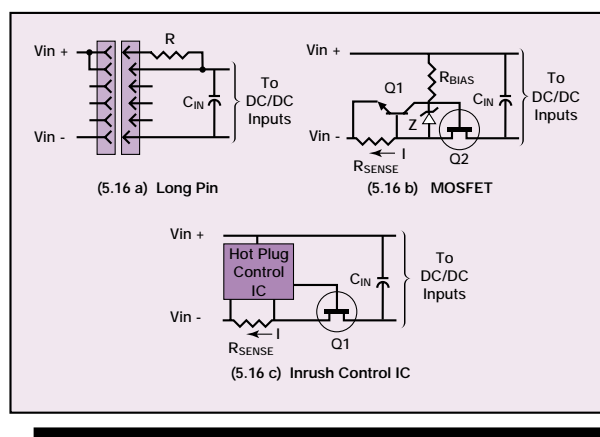


Figure 5.16 - Approaches for Hot Plugging PCB with DC/DC Converters

A second approach uses a power MOSFET to control the maximum current level that is drawn from the intermediate bus. As shown in Figure 5.16b, a simple circuit is used in conjunction with a current sensing resistor to control the MOSFET and regulate the current during inrush conditions. The sense resistor is selected so that Q1 is completely off during normal circuit operation with maximum steady-state current from the intermediate bus. This will drive the MOSFET Q2 into maximum conduction with a fixed voltage drive determined by the value of the Zener diode. If the bus current tries to rise above the normal operating current, such as when the card is hot plugged with discharged input capacitors, Q1 is turned on and robs gate drive from the MOSFET, increasing its on resistance. When operated in this mode, the circuit is a current regulator, with the maximum current determined by the value of the sense resistor. This value of current is then used to charge the input capacitance rather than the much larger unregulated inrush current. The representation shown here is a simplified circuit, and will need to be optimized as appropriate for your particular application. One advantage of this technique over the long pin approach is that it will also limit inrush current when the system is powered up with the circuit board plugged in. It will have slightly less efficiency due to the dissipation in the MOSFET and sense resistor.

The most sophisticated approach is to use a so-called "hot plug controller" IC. These devices are available from suppliers such as Linear Technology, Maxim and Texas Instruments as well as other manufacturers of linear and power ICs. These devices make it easy to accomplish the function of the MOSFET inrush limiter while also incorporating several other features that can enhance the overall power control flexibility of the system. Some of these features include:

- Programmable Current Limit
- Programmable Power Limit
- Programmable Fault Time
- Electronic Circuit Breaker Function
- Ramping of Input Voltage
- "Power Good" Signal Output
- UV Lockout Function
- Easy Shut-down Control

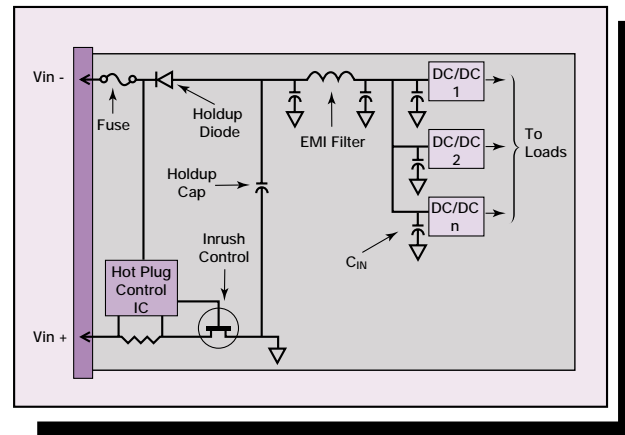


Figure 5.17 - Shared "Front-End" Circuitry on PCB

At most power levels, the ICs will require the use of an external sense resistor and MOSFET as shown in Figure 5.16c. Even so, significant functionality can be achieved with only one IC, one MOSFET, one sense resistor and a few small components for programming the desired features. Consult the applications literature from the IC suppliers for specific features and circuit recommendations.

All of the above discussion about various input functions and circuits may seem overwhelming at first, but it can all actually be accomplished very easily. Most all of the circuitry can be shared between multiple DC/DC converters on the same assembly. This will reduce component count and overall cost. Figure 5.17 shows a PCB containing several DC/DC converters and how one set of input circuits can be shared between them. For purposes of clarity the input circuits are shown drawn to a large scale, but they actually will consume a very small footprint area on the PCB. Note that, in general, each DC/DC converter will have its own small input capacitor located physically close to it.

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5.3 Output Design Considerations

There are a few critical items to keep in mind when designing the output distribution of a power converter.

The voltage tolerance of the load circuits is of course the starting point, and most of the subsequent design issues revolve around making sure that that this tolerance is indeed met under all system operating conditions. Both static and dynamic operational modes must be considered. The static design focuses primarily on making sure that the DC resistance of the distribution system is low enough to meet the circuit voltage tolerances over their range of operating current. Items such as layout and grounding configuration and remote sensing are also involved. The dynamic design is mostly concerned with meeting the circuit requirements during rapid changes in load current. In terms of meeting these requirements, the inductance and capacitance of the output distribution system turn out to be more important than its resistance. These parameters, along with some layout-related considerations, will also influence the EMI characteristics of the system.

Voltage Tolerances - A complete understanding of the DC voltage tolerance of the load circuits is the beginning point for the output distribution design. This step is becoming more critical as the supply voltages for high performance ICs continues to drop - in many cases this supply voltage is less than two volts. A 5% voltage tolerance at 2 volts only allows for a plus and minus 100mV variation in supply voltage. The corresponding good news is that modern DC/DC converters offer truly exceptional voltage regulation performance, including effects of load current, input voltage and temperature. The first step in the distribution design is to determine the allowable distribution drop by subtracting the converter output regulation effects from the allowable

circuit tolerance. The following example will help clarify how this is done.

We will assume a nominal 3.3V requirement with a 5% voltage tolerance and use an Artesyn SXA10 family 3.3V output converter to satisfy the requirement. The required DC voltage at the circuit is $\pm 5\%$ of 3.3V or $\pm 170\text{mV}$. The next step is to determine how much of this total tolerance is consumed by the performance of the converter itself. By referring to the SXA10 data sheet we find a total of four parameters that will affect the static DC output voltage - set point, line regulation, load regulation and temperature coefficient. The data sheet gives worst case values for each of these parameters and an additional typical specification for line regulation and temperature coefficient. In order to be able to make summations of the output voltage variations, they must be all converted into the same units, and we will use $\pm\text{mV}$ for this purpose. For example, the set point is specified as $\pm 1\%$ which will translate to $\pm 33\text{mV}$ for the 3.3V nominal converter. For the temperature coefficient effects, we must know the expected operating temperature range of the converter within the application. Using a temperature range of 25 to 60°C, the specified value of temperature coefficient can be converted to the output voltage variation in $\pm\text{mV}$. Assumptions must be made where no typical specification is given. In the case of output voltage set point, we will assume that the typical value is equal to the worst case value. For the load regulation, we will assume a value of $\pm 7\text{mV}$ rather than the $\pm 10\text{mV}$ worst case value because the range of output load current in the example application is assumed to vary from only 50% to 80% of the converter's operating range. By using these techniques and assumptions, we end up with the data displayed in Table 1. The typical and worst case voltage deviations are summed to arrive at the total expected output

	Typical			Worst Case		
	Spec.	± mV	Notes	Spec.	± mV	Notes
Set Point	None	±33	Assume = w.c.	±1%	±33	
Line	3mV	±1.5		12mV	±6	
Load	None	±7	50-80% load	20mV	±10	
Temp Co.	±0.002 %/°C	±2.3	25 to 60°C	±0.01%/°C	±11.6	25 to 60°C
Total		±43.8			±60.6	
Available		±126.2	170 - Total		±109.4	170 - Total

Table 1

voltage variations. When these values are subtracted from the ±170mV allowed by the circuit, the voltage variation available for distribution effects is determined. Note that in the typical case only 26% of the allowable margin is used by the converter, leaving most of it available for the system distribution.

In practice, the worst case analysis does not usually need to be used. The total worst case value actually makes the additional worst case assumption that **all** of the parameters will be worst case at the same time - a scenario that is not very likely. The system designer will need to make the final judgement about how conservative to be in this regard. Most designers feel comfortable when using typical values obtained from reliable suppliers such as Artesyn. If the application is extremely critical, on the other hand, a worst case analysis is sometimes used to achieve additional assurance of system operating margins. In this example, a total of approximately ±110 to ±130mV is available for distribution system effects.

Static Distribution Design - Designing the distribution system to minimize the DC voltage drops is fairly

straight-forward. It has actually become easier in recent years due to the popularity of DPA systems with the final stage of DC/DC conversion located close to the load circuitry - often on the same circuit board. With these systems, the wide input voltage range of the DC/DC converters does not require ultra-low voltage drop distribution on the intermediate bus. The intermediate bus design is therefore more often driven by transient effects and fault management, as described earlier, rather than by the need to minimize DC losses. Putting the converter on the same board as the load circuits removes connectors and long conductors from the distribution path and results in a very predictable DC distribution environment. We will explain how such DPA DC/DC converter output distribution designs are done shortly, but first we will address the more general topic of DC distribution in centralized systems.

In a centralized system, the DC distribution task can be complex. The output of one converter must often be distributed to several load boards a considerable distance away from the converter. This presents some potential problems:

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- Large DC drops due to distance to load
- Interaction between the load boards
- Voltage drops and unreliability due to connectors

The first issue is normally solved by using physically large conductor sizes along with remote sensing to adjust the voltage to a desired level at one point in the system. We will discuss remote sensing and its limitations in more detail later. These solutions do not come cheaply. The required copper in cables and bus bars, the need for manual assembly, and the complexity of remote sensing all add substantially to the total system cost. Using the proper distribution topology can minimize the interaction issue. Figure 5.18 shows a centralized system with one AC/DC converter supplying power to three load boards. The system is implemented with a **parallel distribution** system in Figure 5.18a. Note how the currents from all three loads appear in the same cable or bus bar.

Since the cable will have a finite resistance, the input voltage to load 3 will change as the load currents in loads 1 and 2 change. The same type of interaction will occur for the other two loads as well. Even using remote sensing will not solve this problem, as it will only be effective at one selected point. This interaction between loads can make such a distribution system totally unusable for systems with low voltage high current loads, especially if the individual load groups are capable of being powered up and down.

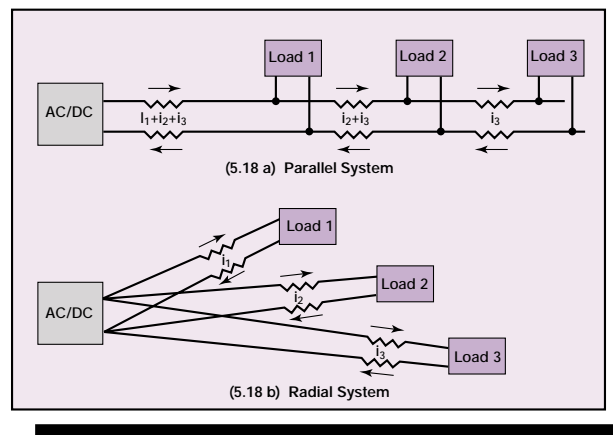


Figure 5.18 - DC Distribution Configurations

A more desirable distribution technique, referred to as **radial distribution**, is shown in Figure 5.18b. Here, each load has its own path to the power converter and will not be affected by changes in load current in the other two loads. Also, the conductor sizes to each load can be adjusted to compensate for its current draw and distance from the centralized converter, maintaining a constant nominal voltage at each of the three loads. As a consequence, the power system will have a much greater probability of meeting its performance requirements if the radial approach is utilized.

We will now look at the DC distribution design for the output of a board-mounted DC/DC converter. Since the vast majority of DPA systems use traces in one or more PCB boards for the final power distribution to the operating circuits, we will assume a PCB distribution technology as opposed to individual wires. Resuming the example we were using previously (3.3V SXA10 application), we will have approximately $\pm 120\text{mV}$ of voltage drop allocated to the distribution system. This allocation must be shared between DC drops and the dynamic voltage variation associated with rapidly

changing load currents. There is no absolute rule-of-thumb as to what percentage to assign to DC vs. dynamic effects, but a good approach is to first calculate the DC drops assuming a robust but cost-effective conductor sizing. Ideally, this should result in the majority of the distribution allowance still available for dynamic effects.

The maximum DC load power will be 80% of the SXA10's 10W maximum rating, or 8W, resulting in a maximum load current of 2.42A. We will first assume a very simplistic DC distribution method - a single-sided PCB with 1oz/ft² copper. The load is 5 inches away from the converter. The voltage and return conductors to the load are both 0.3 inches in width. The total resistance in the distribution system will therefore be represented by a 1oz. copper conductor 0.3 inches in width and 10 inches in length.

The basic expression for calculating the resistance of a conductor is:

$$R = \frac{\rho l}{A}$$

Equation 7

where:

ρ = Resistivity of Copper $\approx 0.67 \times 10^{-6} \Omega \text{ in}$

l = Length of conductor - in

A = Cross Sectional Area of conductor - in²

1 oz/ft² copper has a thickness of 1.35mils (0.00135in).

We now can calculate the total distribution resistance as:

$$R = \frac{(0.67 \times 10^{-6}) \times 10}{0.3 \times 0.00135} = 16.54 \text{m}\Omega$$

This will give a voltage drop of 40mV at 2.42A, which is well within the $\pm 120\text{mV}$ available for distribution effects. Even this modest distribution system meets the system requirements for DC voltage drop. In actuality, it is usually good design practice to use as much copper in the distribution as possible. A dedicated voltage and ground plane is ideal. This will provide several benefits at a modest cost:

- Minimum DC drops and extra margin for dynamic effects
- Additional thermal heatsinking for components and DC/DC converter
- Better EMI environment

For higher power circuits, 2 oz/ft² copper is recommended for the voltage and ground planes. By using a planar design approach the DC distribution system will have maximum performance at very little additional cost. In this example, almost the entire $\pm 120\text{mV}$ would be available for the dynamic performance to be discussed shortly.

There is a convenient PCB resistance calculator available on Artesyn's website as part of their "Virtual Power Laboratory". This tool is recommended as an easier and more complete alternative to Equation 7. You can enter the PCB copper thickness in units of either oz or mils. After entering the expected PCB temperature, conductor width and length, source voltage and load current, the calculator will return values for:

- Voltage Drop in Volts
- Voltage Drop in %
- Voltage at Load

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- Area of conductor in sq. mils
- Resistance of conductor
- Power Dissipated in conductor

By using the calculator, you can quickly evaluate several different distribution alternatives to see their effect on the system performance. You can also see the effects of system operating temperature on the DC resistance and voltage drop performance. There is a similar calculator in the same location, based on conductor sizes in AWG, for discrete wire distribution.

A classic method of overcoming the effects of DC distribution losses is **remote sensing**. In a remote sensed system, the actual voltage at the load is sensed, and the power converter output voltage increased to cancel out the distribution drops between the converter and the load. Remote sensing works very well and is a useful technique, especially for centralized systems with high current levels and large distances between the converter and the load or for high power DC/DC converters in DPA systems. There are some design considerations to keep in mind when laying out your system using remote sensing. Remote sensing lines carry negligible current, so they do not need to be heavy conductors. They can be susceptible to noise, however, so careful layout practices should be used, including:

- Keep the impedance low to reduce noise pickup. Run the sense conductors close to each other and over a ground plane.
- In a discrete wiring situation, use twisted pair for the sense lines.
- Install a small (100nF) capacitor across the sense lines at the sense point.

Remote sensing does, however, have some disadvantages. It will increase the complexity of your system in the following ways:

- Need for two more distribution conductors (sense lines)
- Only regulates voltage at one point - concern for multi-board systems
- Additional system failure mode
- Difficult fault diagnosis
- Affects converter stability analysis
- Increased output voltage at converter increases voltage stress on capacitors and reduces reliability
- May cause nuisance tripping of Overvoltage detector if used in conjunction with upward voltage trimming

If one of the sense conductors opens during system operation, the converter output voltage will increase. The extent of this increase is usually limited by circuitry internal to the converter, but it can still create an awkward situation for efficient fault diagnostics and repair. It is difficult, even for skilled service personnel to distinguish between a converter fault and an open sense line.

The stability analysis item may require additional explanation. In a normal locally sensed converter, the output voltage is measured at the output of the converter's output filter and fed back to the converter's control circuitry. All of the components within the converter's feedback loop are thus known to the converter designer, and are used to ensure that the converter will be stable over all combinations of line voltage, load current and external capacitance. When remote sensing is used, the feedback sensing point is

moved to the remote sensing location. All of the system distribution components are then contained within the converter's feedback loop. This will include capacitance and series inductance. Since the converter designer has no exact knowledge of the actual components now included in the feedback loop, the converter becomes more susceptible to instability if extreme values of distribution components are used.

Artesyn makes several converters with remote sensing capability, and they are good choices for centralized systems or for situations with heavy currents and the need for precise voltage settings at a remote point. In general, however, it is recommended to first determine if a solution without remote sensing is possible. If so, the power system can be significantly simplified. With the current trend toward DPA and on-board DC/DC converters, the need for remote sensing is definitely decreasing. Artesyn's SimScope simulation tool will enable you to easily configure systems with and without remote sensing for the supported converter types and determine how that design choice affects the system performance. Remote sensing can be easily disabled by just jumpering the remote sense pins to the converter output pins with PCB traces at the converter.

Another design technique, that achieves much of the same results as remote sensing without the disadvantages, is **voltage trimming**. Many modern DC/DC converters have the ability to adjust their output voltage either upward or downward by the addition of a single external resistor. If the nominal distribution drop to the load is known, it can be offset by increasing the converter voltage by the corresponding amount. Unlike with remote sensing, the load voltage will vary slightly as the load current changes, but the average voltage at the

load can be set to any desired value. In our previous example, the converter output would be set 40mV high (3.34V) and the load voltage would be 3.3V at the 2.42A maximum load. This would make the entire $\pm 120\text{mV}$ margin available for dynamic variations. Artesyn's Virtual Power Lab contains a calculator for automatically determining the trimming resistor value to use with Artesyn's DC/DC converters for any desired output voltage. There is also a calculator for selecting the closest standard resistor value to the calculated resistance. In our example, the voltage trimming calculator returns a resistor value of 53.825Ω , and the standard value calculator gives a value of 53.6Ω with an error of 0.42%.

Dynamic Distribution Design - The AC performance of the power system will be determined by the combination of the high frequency impedance of the DC distribution network and the dynamic performance of the power converter. From a load circuit point of view, the two primary criteria for a successful dynamic design are control of high frequency noise content on the power planes and the ability of the power system to deliver sufficient transient energy to allow for rapid load current changes. This is aided by designing the DC distribution network to have low impedance from DC to the highest load circuit operating frequency.

There are two sources of high frequency noise on the power planes - converter switching noise and circuit operating noise - and they are both controlled by proper DC distribution design. Converter switching noise will occur in bursts that coincide with the converter's output ripple frequency. It will be attenuated in a properly designed distribution system due to the distributed inductance and capacitance of the distribution network

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acting as a low pass filter. Circuit switching noise is caused by the voltage drop across parasitic inductances in the circuit packages as the individual circuit elements change state and force current through the inductive elements. This is a much more distributed effect than the converter noise, since it occurs at all points in the load circuits, often at different frequencies and times. The key to keeping the circuit switching noise localized and not propagating throughout the system is to have sufficient high frequency decoupling capacitance located directly adjacent to the circuits.

To meet the high frequency power demands of the load circuits, energy must be delivered to the load when it is needed - often in a time period of nanoseconds. Unlike an idealized power source with infinite frequency response, any power converter will have a finite bandwidth which will limit its ability to source large transient energy demands on short notice. The response time of the converter will be limited by the bandwidth of its control loop. For present day isolated DC/DC converters, this upper frequency will be in the range of 3 to 10kHz. For non-isolated high slew-rate converters the upper frequency could extend a decade higher, to perhaps 30kHz. This is clearly insufficient to meet the demands of many types of load circuits, which may require their energy in nanoseconds, not in tens or hundreds of microseconds.

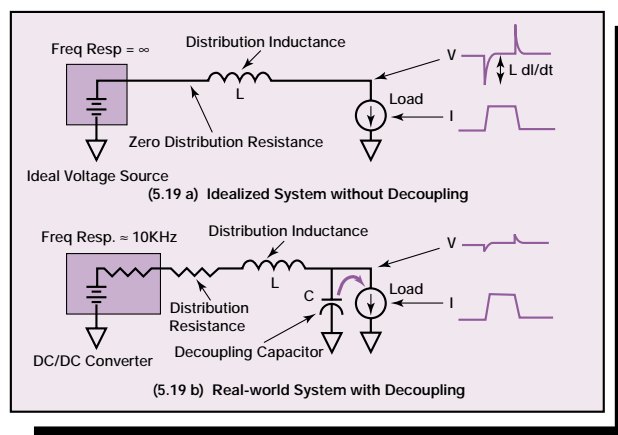


Figure 5.19 - Power System Dynamic Performance

At first it may seem that developing faster power converters is the answer. But let's assume, for the moment, that we could design a **perfect** power converter that looks like an idealized battery source with zero internal impedance and infinite frequency response. When such a converter is put into an actual real-world system, as shown in Figure 5.19a, we can begin to see the limitations of solving the problem with just improvements to the converter's response time. In Figure 5.19b, we show an ideal voltage source providing power to the load through a distribution system. For illustration purposes, we will assume zero resistance in the distribution network and no decoupling capacitance. We show the distribution inductance, L , which will be present in any system due to the non-zero distance between the power source and the load. When changes in load current occur, there will be a voltage drop across this inductance, determined by $L di/dt$. As seen in the figure, this will result in voltage deviations at the load, and the idealized voltage source is no longer ideal as far as the circuit is concerned! Without more localized sources of energy near the load, even an idealized power source will not meet the system's requirements.

The universal solution to this problem is the usage of decoupling capacitors, as shown in Figure 5.19b. The decoupling capacitor, C, provides a local source of energy for the circuit, and furnishes the needed high frequency transient energy. Now the circuit's requirements can be satisfied even with a non-idealized distribution system containing resistance and a real-world power converter with a non-zero source impedance and a limited bandwidth. This is encouraging!

Figure 5.19b shows an ideal capacitor element, which of course does not exist. There is always some equivalent series resistance (ESR) and equivalent series inductance (ESL) internal to the capacitor's structure and its interconnection to the circuit board. Even if the capacitor is mounted physically right next to the switching circuit, there is still some finite distance between them with some value of interconnection inductance that will prevent the capacitor from acting as an ideal circuit element even for a brief period of time. The behavior of this series circuit, consisting of C, ESR and ESL, must be understood in order to get a good intuitive feeling for the operation of the decoupling capacitor network.

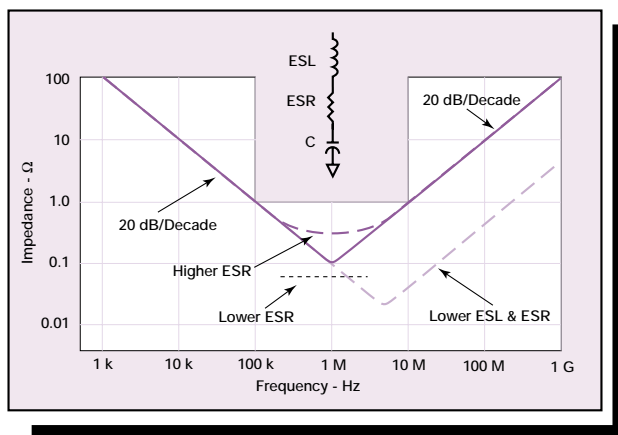


Figure 5.20 - Decoupling Capacitor Impedance vs. Frequency

Figure 5.20 shows the circuit and a plot of its impedance as a function of operating frequency. The three elements form a series resonant circuit, with the frequency of resonance determined by:

$$f = \frac{1}{2\pi\sqrt{ESL \cdot C}}$$

Equation 8

At resonance, 1MHz in this example, the total of the three elements appears resistive with an impedance value equal to ESR, 0.1 Ohm in this case. Lower values of ESR will not benefit this circuit if C and ESL remain the same. Higher values of ESR will broaden and raise the impedance near resonance. At frequencies lower than resonance, the circuit appears capacitive, with impedance that rises 20dB for each decade of frequency below resonance. Above resonance, the net effect is inductive. In this region, the impedance can still be low and beneficial in terms of noise control, but we cannot depend upon it for a source of energy to supply our circuit's transient current needs. So we always want to operate in the left-hand region where the circuit element is capacitive, but we also want a low value of impedance from DC up into the MHz range. Clearly, the one circuit shown in Figure 5.20 cannot accomplish this. If we find a capacitor with ultra-low ESL and ESR, the resonant frequency will rise and we will have a capacitive characteristic with a lower impedance over a broader frequency range, but still too much impedance at the lower frequencies. This possibility is shown by the dashed line response characteristic in Figure 5.20. There is no single type of capacitor that provides enough C at low frequency combined with ESR and ESL low enough to handle the higher frequencies. The solution is to use more than one size or type of capacitor to handle the entire frequency range. They can include:

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- Low frequency "Bulk" electrolytics ($>10\mu\text{F}$)
- Mid Frequency Tantalums or Ceramics (0.1 to $10\mu\text{F}$)
- High Frequency Ceramics (0.001 to $0.01 \mu\text{F}$)
- Printed Circuit Board Layer-to-Layer Capacitance

This approach, along with the power converter's ability to handle the lower frequency demands, will result in a reliable source of energy over the complete desired frequency range as shown in Figure 5.21. Note that there are at least two sources of energy at every frequency above 1kHz. This overlapping arrangement of different types of decoupling capacitors provides for the best assurance that your system will operate reliably with low noise levels and good dynamic performance.

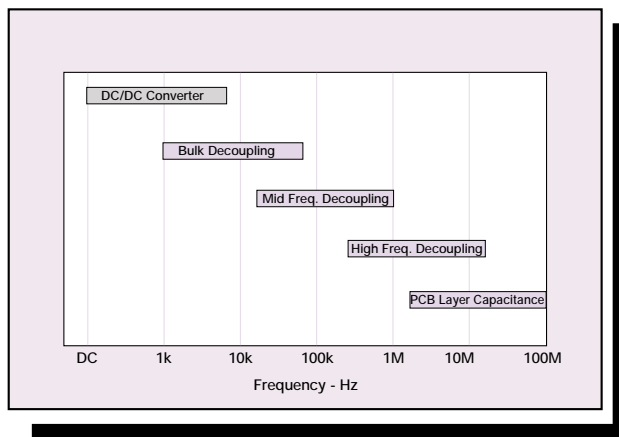


Figure 5.21 - DC Distribution Energy Sources vs. Frequency

One of the key techniques for improving the performance of decoupling capacitors is paralleling several of them. Because capacitance in parallel is additive while inductance and resistance in parallel results in smaller values, paralleling capacitors has big dividends. For example if 10 identical capacitors are paralleled, the total capacitance will be ten times the value of the capacitor, while the ESR and ESL will be one tenth of that of the

individual capacitor. Note, however, from equation 5.8, the resonant frequency will remain the same. An example is shown in Figure 5.22, that plots the impedance of a single 1mF capacitor and the impedance of ten of them paralleled. Note that the resonant frequency, about 9MHz in this case, remains constant. If an impedance of one ohm were the goal for the power system impedance, we can see how the effective decoupling bandwidth (frequency range over which the impedance is below the goal) is now much broader. For this reason, most decoupling systems will utilize several capacitors in parallel, which also has the advantage of putting some capacitance closer to all of the load circuits so that the interconnection inductance is minimized.

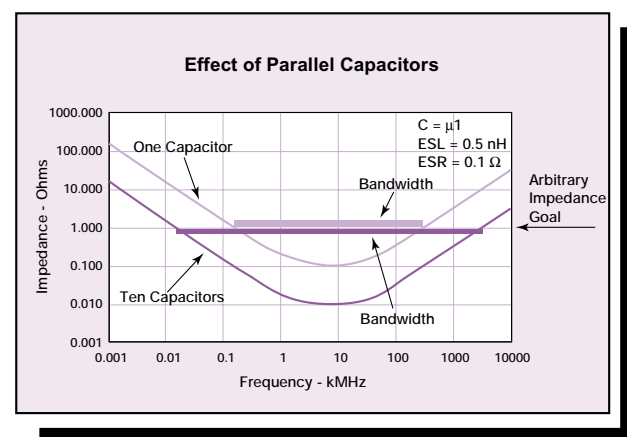


Figure 5.22 - Increasing Decoupling Bandwidth with Paralleled Capacitors

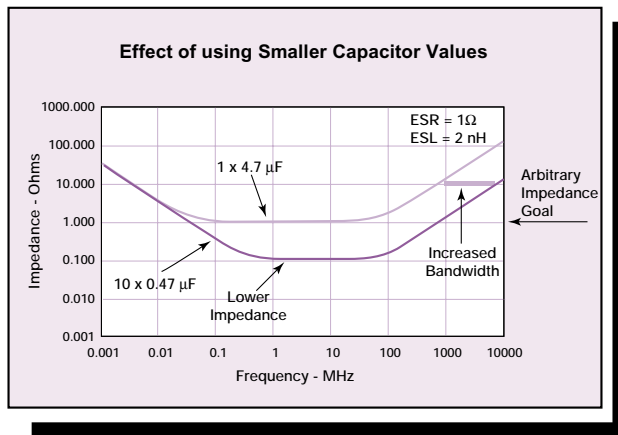


Figure 5.23 - Increasing Decoupling Bandwidth with Small Capacitor Values

It can also be beneficial to use a larger number of smaller capacitor values to achieve the desired total capacitance. In this case, the resonant frequency will go up because of the smaller total ESL, but the decoupling bandwidth will increase. See Figure 5.23 for an example, and note the lower impedance and extended bandwidth. Normally we try to minimize ESR, but it can actually be helpful in some cases. Figure 5.24 compares the characteristics of tantalum chip capacitors with ceramic chips. The ceramic parts have a lower ESR, which is often helpful, but note how the tantalum actually gives a broader region of good decoupling performance even though its ESR is higher. Relying solely on ceramic capacitors can therefore sometimes result in missing regions of decoupling coverage and in "peaky" impedance curves due to the high Q resonant circuit of the ceramic capacitor. This effect can be minimized by depending upon the ceramic capacitors for only the higher frequency range and by using more than one value of ceramic capacitance.

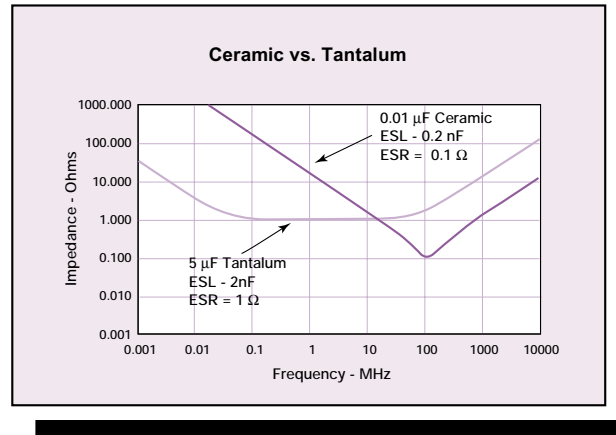


Figure 5.24 - Tantalum and Ceramic Chip Characteristics

The best solution, as mentioned previously, is a combination of more than one type of capacitor with several of each type paralleled for reduced ESL and ESR. As an example, we have shown a possible decoupling system for a large high-powered circuit board in Figure 5.25. It shows the usage of aluminum, tantalum and ceramic capacitors in a total of 4 values. This, in conjunction with the converter's output impedance at low frequency and the PCB layer-to-layer capacitance at high frequency results in an overall distribution system impedance of around 10 milliohms or less from DC to 1 GHz. There are several available choices for dielectric type for ceramic capacitors. For decoupling usage, the best choice is most often the X7R dielectric. The higher quality devices in this category will have a very high volumetric density, wide capacitance range and an acceptable ESR.

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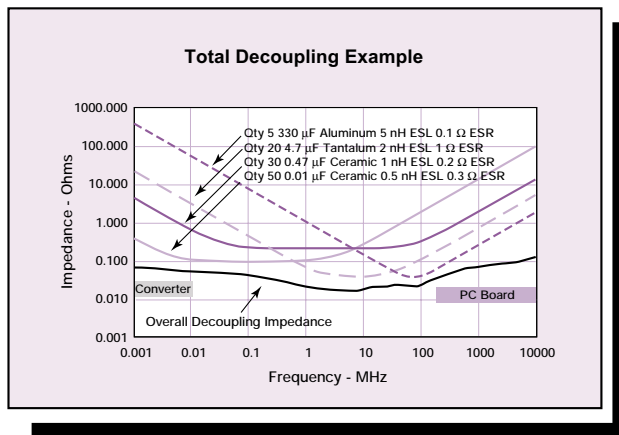


Figure 5.25 - Total Decoupling System Example

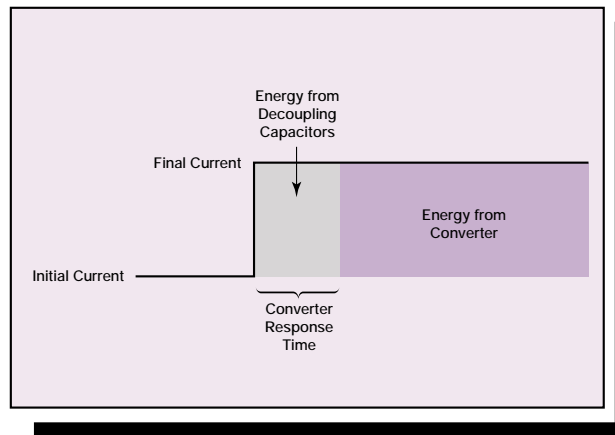


Figure 5.26 - Energy Sources During Load Transient

The amount of capacitance required to achieve the desired dynamic performance will be dependent upon the dynamic current of the load and the response time of the power converter. We can calculate the **minimum capacitance** value by using the same equation (5.4) that we used to determine the value of a holdup capacitor. In this case:

$$C = I \frac{dt}{dV}$$

where:

C = Minimum Capacitance

I = Transient Load Current

dt = Converter Response Time

dV = Allowable Voltage Drop

The intent is to have enough capacitance close to the load to supply the transient energy until the converter can begin to supply the additional current, as shown in Figure 5.26. Returning to our example using the SXA10 DC/DC converter, suppose that the transient load current change is 0.5 amps. We have $\pm 120\text{mV}$ available for dynamic effects, so that will determine the allowable voltage drop, dV. From the SXA10 data sheet, we find that the maximum transient recovery time of the converter is $200\mu\text{s}$. The minimum capacitance can then be calculated to be:

$$\text{Minimum Capacitance} = 0.5 \times \frac{200 \times 10^{-6}}{0.12} = 833\mu\text{F}$$

This capacitance can be distributed throughout the distribution system, including the output capacitance of the converter, but having at least some of it near the load will be beneficial so that the inductance between the capacitance and the load is minimized. In addition to the voltage decrease that is a function of the amount of decoupling capacitance, there will be an initial voltage transient that is determined by the inductance of the decoupling capacitance and the inductance between the

capacitance and the load. The maximum allowable inductance is determined from:

$$L = V \frac{dt}{di}$$

Equation 9

Where:

V = Allowable voltage drop

dt = Transient current ramp time

di = Transient current

In our example, if the ramp time of the transient is $0.5\mu\text{s}$, the maximum allowable inductance is then:

$$L = 0.12 \times \frac{0.5 \times 10^{-6}}{0.5} = 120\text{nH}$$

A generalized transient voltage response, showing the effects of both decoupling capacitance and inductance, is given in Figure 5.27. Note that higher values of capacitance will decrease the voltage droop after the inductive spike, but that the recovery to the nominal value will be longer.

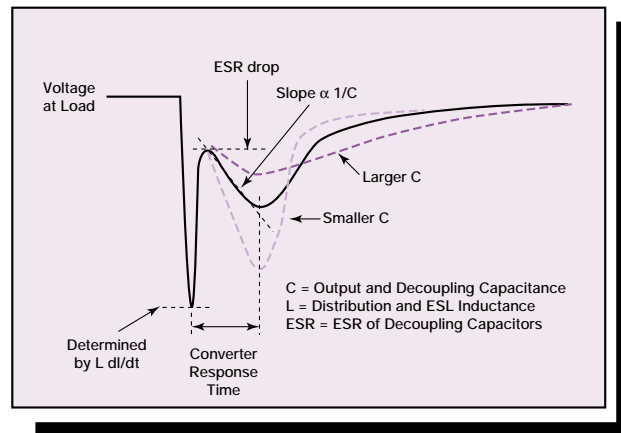


Figure 5.27 - Generalized Transient Voltage Response at Load

There are also practical limits as to the **maximum capacitance** that should be used in a distribution system. Cost, of course, is one consideration. But the power converter stability will be affected by the amount of capacitance on its output, and there is a maximum limit for which stability will be guaranteed. In the case of the SXA10 as used in the above example, the data sheet indicates a maximum of $6600\mu\text{F}$, which is considerably more than required for good dynamic performance. If the data sheet for the converter you are using gives no value of maximum capacitance, $100\mu\text{F}$ per amp of output current is usually a safe value.

We have so far only considered the ESR and ESL internal to the decoupling capacitors. Attaching the capacitors will add additional resistance and inductance in terms of lead length, with the inductance the more troublesome parameter, so the capacitor attachment layout will affect the overall performance. The good news is that modern SMD technology has eliminated the large inductances that were associated with axial lead capacitors. Even with the leads trimmed as short as possible, the lead inductance of these devices was at least 3nH . By comparison, the interconnect inductance of SMD chip

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capacitors is in the range of 0.5nH to 1.2nH. This will be a function of the capacitor's physical size and orientation (interconnect on long or narrow side). PCB traces that interconnect the capacitor pads to the vias connecting them to the ground and voltage planes should of course be made as short as possible. As a rule of thumb, PCB traces will be about 10nH per inch for multi-layer boards and 20nH per inch for single-sided boards. Figure 5.28a summarizes these layout considerations. In the case of multi-layer boards used in high frequency systems, the side of the board you use to mount the decoupling capacitors can even make a difference. If the voltage and ground planes you are decoupling are located near one surface of the board, the capacitors should be located on the same side. As shown in Figure 5.28b therefore, this will result in shorter interconnection lead lengths and better high frequency performance.

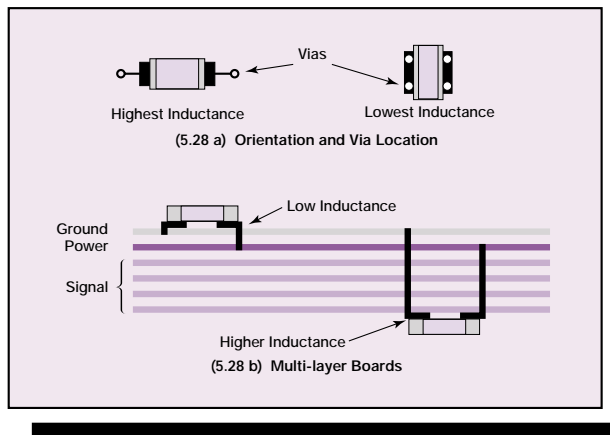


Figure 5.28 - Decoupling Capacitor Layout Considerations

The SimScope simulation tool on Artesyn's Virtual Power Lab website is recommended as an easy way to design and verify decoupling systems. It has a transient response analysis function with which you can enter any load current transition and see the result on the DC voltage at the load. You can then vary the assumptions

for the amount of capacitance and inductance in the distribution system as well as the ESR and ESL of the decoupling capacitors and determine their effects. Unlike the simplistic analysis we presented above, the SimScope tool will include the actual modeled response of the power converter, including the effects of the capacitance internal to the converter on its output filter.

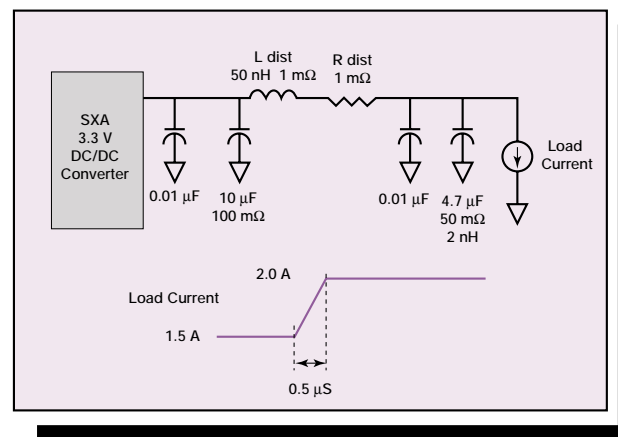


Figure 5.29 - SimScope Simulations Set-up

As an example of its use, see Figure 5.29. Here we have modeled the SXA10 converter system we have been using as an example. The load current transition is set to be 0.5A in 0.5µS, or a 1A/µS slew rate. The converter's output capacitor will provide most of the bulk decoupling, with only 10µF added externally. The distribution inductance is assumed to be 50nH. One milliohm is assumed for distribution resistance and another milliohm internal to the inductance. A 4.7µF capacitance is assumed to be near the load, probably composed of two or more paralleled capacitors, giving an overall ESR of 50ΩW and an ESL (including interconnections) of 2nH.

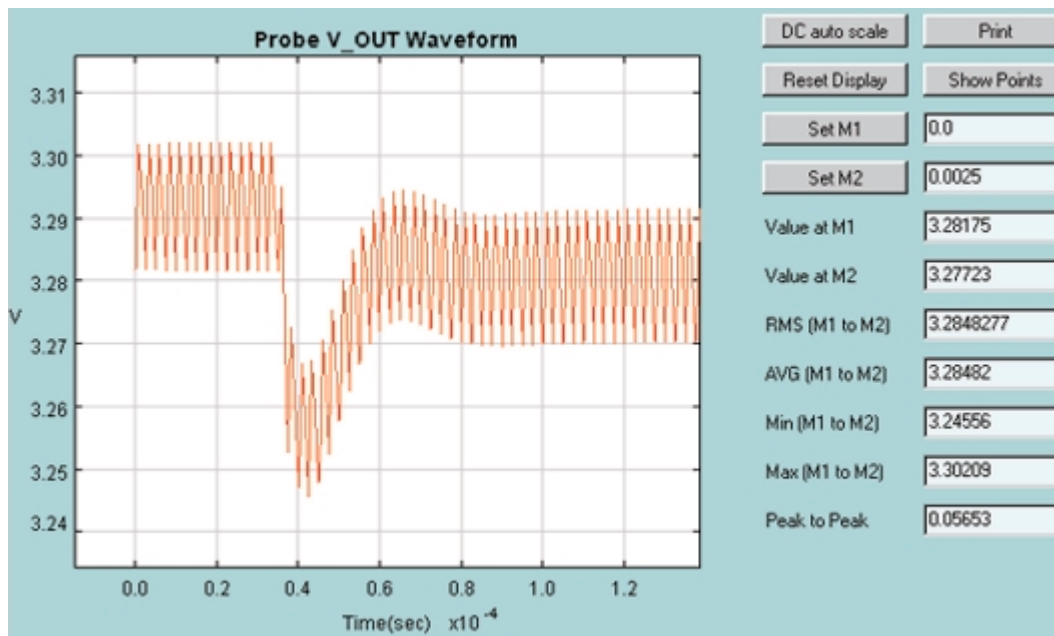


Figure 5.30 - SimScope Simulation Result

The simulation results are shown in Figure 5.30. The total voltage deviation is only 54mV, well within the 120mV allowance in our assumed example. Also note that the actual converter response time is only on the order of 20 μ S, much faster than the specification. Using SimScope in such a fashion should increase the confidence in your power system design and perhaps relax some of the worst-case assumptions made in the course of the preliminary analysis.

Grounding and Isolation - One of the basic design decisions will be whether to use isolated or non-isolated DC/DC converters. The type of system you are working with and the design standards of your particular organization will influence this decision. However, there is often room for some flexibility, especially at the level of the final circuit card. In the case of board-mounted DC/DC converters where all of the converter output

power is contained to the same circuit board, you have a high level of control over isolation and grounding effects.

In power architectures with the same voltage level supplying multiple circuit boards in different physical locations, much more care must be taken with grounding considerations.

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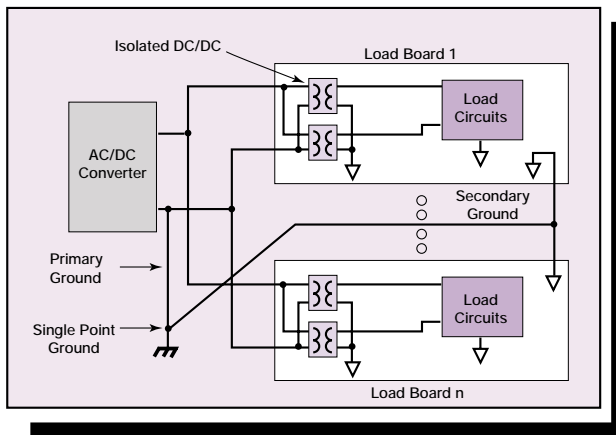


Figure 5.31 - Single Point Grounding System

The main advantage of isolated converters (other than adherence to any required safety considerations) is that you can control the currents flowing in the secondary circuit. With a non-isolated converter, the input and output grounds will be common, and currents from other circuits connected to the input can find their way to the secondary and possibly interact with and upset the load circuits. The ideal situation will be a "**single point ground**" system, where the load circuit return is connected to the system's reference grounding point by a single conductor. One example of such a system is shown in Figure 5.31. Note that the primary and the secondary returns are connected to each other at a single point. This will prevent ground current flowing in either connection from causing a voltage drop in (and interaction with) the other ground system.

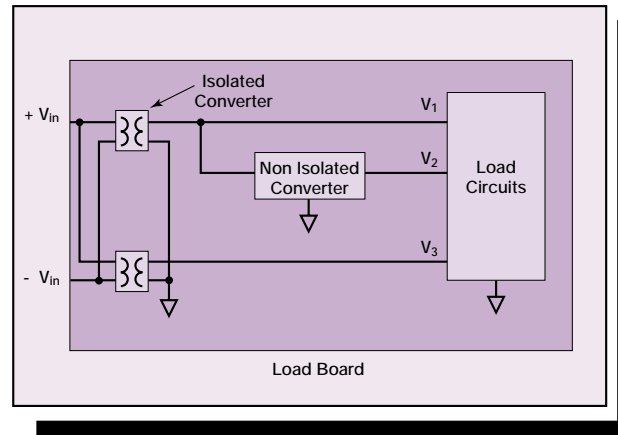


Figure 5.32 - Usage of a Non-isolated Converter in a DPA System

It is possible to use non-isolated converters while maintaining a single point ground system. This is often done for the purpose of generating low power levels for usage within a circuit board using an isolated DC voltage as the source. Voltage Regulator Modules (VRMs) used in personal computers are one example. Non-isolated converters can also be used in more classical DPA systems, as shown in Figure 5.32. In this example, the isolated output of the a DC/DC converter (5V, perhaps) is used to generate a low power level such as 1.8V. This could be done with either a non-isolated DC/DC converter, a discrete switching converter circuit using an integrated control chip, or a linear regulator. In any case, the usage of such a non-isolated device will not compromise the overall system grounding philosophy or prevent the usage of a single point ground system.

Noise Control and EMI - The usage of a proper decoupling and grounding system as described above is the most important step you can take to insure that your system meets its EMI objectives. The decoupling network will create a low impedance path for differential-mode noise from the converter output and prevent it from

radiating within the equipment enclosure. Usage of isolated converters will allow for segregation of input and output return currents so that any required common-mode filtering can be easily applied. With good design practices, most systems should not encounter any significant EMC problems that are related to the secondary power system design.

The layout of the PCB in the area of the power converter can have either a positive or a negative influence upon the EMC performance of the system. One goal is to keep any electromagnetic fields generated by circuitry within the power converter confined to as small an area as possible. This will lessen their influence on surrounding circuitry. The best way to do this is to use a continuous ground or voltage plane in the PCB directly under the converter. Ideally, a plane referenced to the input return should be used under the input side of the converter and a secondary referenced plane under the output side. A generalized example of this technique is illustrated in Figure 5.15. It can be used with either multi-layer or single-sided circuit boards, but there is more design flexibility and more copper available with multi-layer boards. When implementing this portion of the PCB design, it is important to keep in mind the safety criteria such as the creepage and clearance spacings between planes referenced to the primary and secondary circuits. More information on the safety-related design criteria can be found in Chapter 10, and recommendations on specific PCB layouts are contained in the applications literature for many DC/DC converters. EMC issues will be discussed in more detail in Chapter 9.

5.4 System Control and Diagnostics Considerations

In Chapter 2 we discussed the diagnostic signals and control features that are included internal to the latest power converter products. These capabilities provide a considerable level of system protection and flexibility. In this section we will see how these converter functions can be integrated into an overall system-level control and diagnostics strategy. We will discuss the control and sequencing of multi-level power systems and also recommendations for a system diagnostics strategy as a function of the power architecture.

Controls - In a DPA system using distributed DC/DC converters the remote on/off control signal for the converters will usually be referenced to the intermediate bus voltage return. Since it is desirable to isolate this return from the secondary voltage return, one of the major decisions to be made is whether to locate the control circuitry on the primary or on the secondary side of the converter. Primary side control is easier in that there needs to be no isolation to drive the converter on/off input. This can be convenient if you want to configure the converters to turn on and off automatically in the presence or absence of the intermediate bus voltage or if you are using a primary-side controller without feedback from the secondary side. See Figure 5.33.

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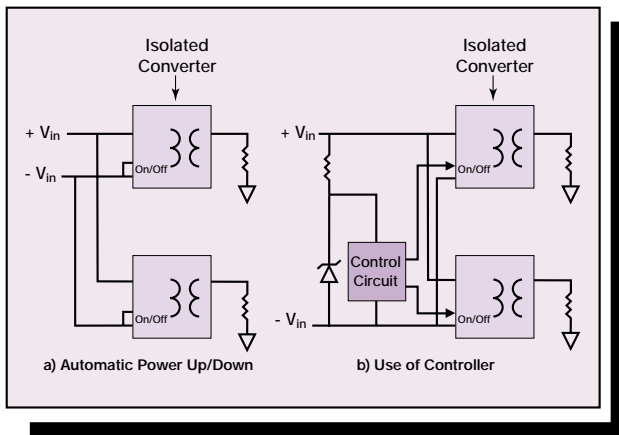


Figure 5.33 - Primary-Referenced Control Systems

Secondary side control is sometimes used if it is desired to utilize information from the secondary of the converters, such as output voltages, sensed currents, etc., to control the converters. This allows for additional flexibility but will require some kind of auxiliary isolated voltage to power the control circuits. Isolation must also be provided between the control circuit outputs and the primary-referenced remote on/off inputs. This is usually in the form of an optocoupler or relay contact closure. A generic configuration for a secondary referenced control system is shown in Figure 5.34.

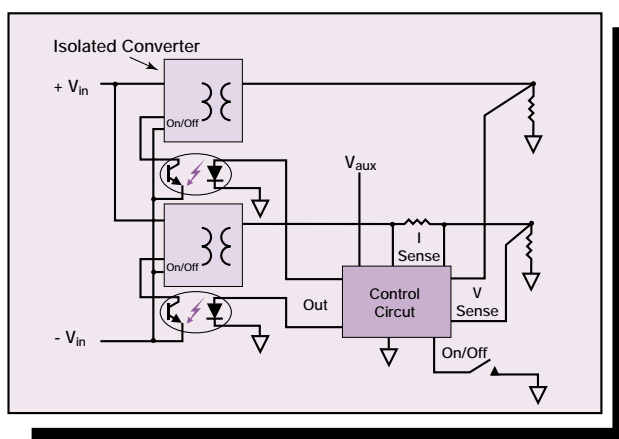


Figure 5.34 - Secondary-Referenced Control System

Voltage Sequencing - When a system operates from more than one voltage level, there is often a need to control the sequence in which the voltages are applied and removed. One common application of voltage sequencing is to prevent substrate currents and possible latch-up conditions if an integrated circuit operates from two voltages and the lower voltage becomes more positive than the higher one. This could happen if the converter supplying the lower voltage is turned on before the converter supplying the higher one. To prevent these types of conditions from occurring, the two power sources could be powered up in a prescribed order, which is referred to as sequencing.

If you are in a situation that requires sequencing, the first item to establish is the turn-on characteristic of the power converters you are going to use. Any power converter will exhibit a finite time interval from the time its on/off control signal is activated to the time when the output voltage is within specification. This time period is composed of two parts - the delay time and the ramp-up time. The delay time is the time that it takes for the converter to begin operation, which is usually on the order of a few milliseconds. All but the most basic converters will ramp the output voltage in a smooth fashion rather than having the output increase as quickly as possible. This is done to allow the output capacitance to charge without putting the converter into an overcurrent condition. These ramp times are usually in the range of 5 to 50 milliseconds. The total start-up time, from turn-on to output within regulation limits, can be from 10 to 100 milliseconds. This type of information should be contained in the data sheet and applications literature for the converter. Be aware that ramp times are usually specified assuming a resistive load. If you have large amounts of capacitance on the output of the converter, the ramp time could increase. Consult the

converter manufacturer if you need more information.

One method that is sometimes used to prevent the back-biasing of a voltage level without resorting to actual sequencing of the converters is to use a diode clamp between the voltages as shown in Figure 5.35a. In this example, assume that the circuit specification requires that the 1.8V level never be more than 1V more positive than the 3.3V level. Ideally, the 1.8V level could be applied first, and then the 3.3V level. Or, they could both be ramped up simultaneously. Instead, the diode is installed. Now, if the 1.8V level is turned on first, it will raise the level of the 3.3V input also and not violate the circuit specification. After the 3.3V supply comes up, the diode is reverse biased and effectively out of the circuit. While this approach will work as far as this particular circuit requirement is concerned, note that it can apply a bias to the 3.3V supply output before the 3.3V supply is turned on. Depending on the design of the 3.3V converter, this could modify its turn-on behavior or perhaps even damage it. Therefore always check with the converter manufacturer before using this type of diode clamping approach for sequencing.

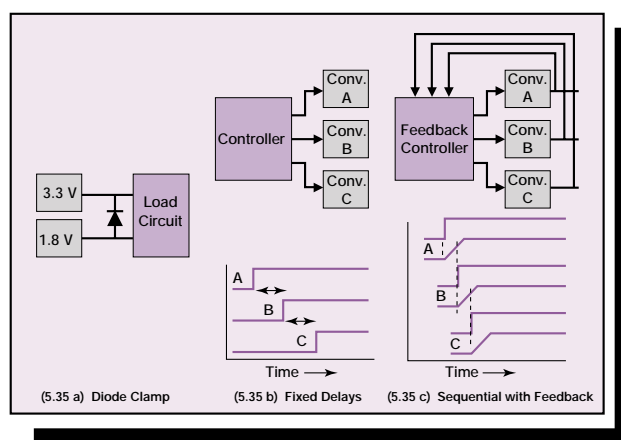


Figure 5.35 - Sequencing Methods

The easiest form of actual sequencing is to supply delayed power-on commands to the converters from some kind of control circuit as shown in Figure 5.35b. The delays can be programmed by means of RC time constants, since they will be long and somewhat non-critical. Since there is no feedback to the controller from the outputs of the converters, the sequencing will continue even if one converter has a problem unless there is additional system-level diagnostics to verify that all of the converters become operational. Figure 5.35c shows a method whereby feedback to the controller can be used to insure that each converter comes up before the next one in the sequence is activated. Thus the controller serves a dual purpose - verifying converter operation and sequencing. The verification is usually done with simple comparator circuits using a reference voltage internal to the controller circuit and set to trip at the regulation limit of each voltage level. This method can result in shorter overall power up sequencing times since there are no extra delay margins inserted into the sequence.

The controller circuits can be custom analog designs using conventional comparators, op amps and discrete components. It is also possible to use the new and highly integrated "Power Supply Supervisory Circuits" (SVS). This can be a convenient and inexpensive way to accomplish both sequencing and other control and diagnostic functions. We have presented this discussion assuming the usage of individual converters for each voltage level. In practice, it is often possible to use a dual or triple output converter instead. The EXB30D DC/DC converter, available from Artesyn Technologies, provides two such positive sequenced outputs. In this case, the sequencing task is usually much simpler since the relationship between the voltage ramps of the converter outputs will be established by the converter

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manufacturer - usually in a way that is compatible with the most common load circuitry. This information should be available from the data sheet and applications material for the converter.

The power down sequencing should not be ignored. The same control methodologies can be used as when performing the power up sequence. There will be the additional consideration of the decay time for each voltage level. The decay will begin with the shutdown of the power converter, but the length of the decay will be a function of the amount of capacitance on the voltage level and the system circuit impedance vs. voltage level. This type of analysis should be done for both the normal controlled power down sequence and an uncontrolled loss of input power.

Fault Diagnostics - Diagnostics can be a challenging design task, especially with centralized architectures, if every eventuality is to be considered. The complexity, cost and failure rate of the diagnostic system can soon exceed that of the power generating elements themselves! So moderation is the key when designing diagnostics. The goal is usually to get the system operational with minimal downtime. To achieve this, it often makes economic sense to not pursue the ultimate level of fault analysis but rather to replace one or more entire assemblies even if only one of them contains the failed component. As we will see, the diagnostics tends to be much less complex with DPA systems, with board-mounted power being particularly easy.

The most common types of faults in distributed power systems are, in rough order of frequency, as follows:

- Overcurrent or short in load circuit
- Loss of fan, airflow or over-temperature shutdown
- Intermediate bus voltage fault
- DC/DC converter primary failure / blown fuse
- DC/DC converter fault giving low output voltage
- DC/DC converter fault giving overvoltage output

Trying to isolate each of these fault types completely will require measurement of voltages and currents at several places in the power system. Current measurement, in particular, tends to be expensive, unwieldy and an addition to the overall system failure rate. Note in the following table that each of the above failure types, with the possible exception of over-temperature faults, ultimately results in an easily measured deviation in output voltage from the normal regulation range. It is recommended therefore that the diagnostic effort concentrate on measuring voltage, especially if system repair rather than analysis is the primary focus.

Fault Type	Result
Over Current Constant Current Foldback Latched Shutdown/Auto Retry	V_{out} Low V_{out} Low V_{out} Zero, Converter off V_{out} Zero Periodic Retry
Over Temp - Fan or Airflow Loss OT Shutdown in DC/DCs No OT Shutdown	V_{out} Zero, Converter off V_{out} Normal, failure rate higher
Intermediate Bus Fault UV/OV Lockout No UV/OV Lockout	Bus Volt. High or Low, V_{out} Zero Bus. Volt. High or Low, V_{out} High or Low
DC/DC Primary Fault/Blow Fuse	V_{out} Zero
DC/DC UV Fault	V_{out} Zero
DC/DC OV Fault No internal OV Protection OV Protection	V_{out} High V_{out} Zero

Table 2

There are many possible diagnostic outputs available from DC/DC converters from different manufacturers. These outputs will have different value to the system designer dependent upon the system's diagnostics and repair philosophy. We will offer some general assessment here as to their usefulness, but the final judgement will be with the power system designer. Remember that for each additional fault indicator pin coming from the DC/DC converter, there will need to be additional system wiring, circuitry and possibly indicators.

The most basic and important form of protection is overcurrent. This is offered in almost all DC/DC converters. There are really two aspects to the overcurrent implementation - primary and secondary. Primary protection is provided by the fuse in front of the DC/DC converter and protects the system wiring from possible high current levels resulting from a fault that shorts the intermediate bus voltage. The secondary overcurrent protection is usually electronic in nature and is designed to protect the load circuitry and wiring in the event of an overload by the circuitry of a short circuit fault in the secondary distribution network. It is assumed that some form of converter overcurrent protection is used in all the examples presented here. There are several types of implementation of the secondary overcurrent protection as shown in the previous table. All of them, however, ultimately result in the output voltage of the converter going low so they can be accommodated by the same basic system diagnostic strategy.

Overvoltage protection has been a feature of converters for decades now. At one time it was essential because one converter would power several boards or an entire

system and an overvoltage fault could destroy thousands of dollars worth of circuitry in a centralized power system. In a DPA system, a DC/DC converter will power a smaller set of load circuits, so the economic consequences of an overvoltage fault will be much less severe. With board-mounted DC/DC converters, the system repair philosophy is often to replace the entire board rather than replacing the failed converter, so damage to circuitry may not actually represent a "real" cost. If the boards are repaired or renewed after replacement, then the incremental cost of providing overvoltage protection within the power converter(s) is probably a wise expenditure. Converters for shelf-level systems will almost always contain overvoltage protection as will the Front-End converter that generates the intermediate bus voltage.

With most DPA systems, the most frequent overvoltage fault will be "soft" faults due to the usage of isolated DC/DC converters with transformer isolation of the secondary from the primary. There will be no direct path from primary to secondary that could dump the full low impedance DC supply voltage directly to the load even in the event of a catastrophic short of a switching semiconductor. Instead an overvoltage fault would be:

- Marginal increased output voltage due to value change in feedback network or open remote sensing line.
- Transient overvoltage due to inductive switching in load circuit.

Because of the above type of considerations, overvoltage protection is usually used in higher power converters but sometimes omitted in low power (<20W) offerings for card-level systems. It can also be implemented at the

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system level by sensing the voltage at the load and inhibiting the converter via its remote on/off input if the voltage gets too high. Some converters will use a transient voltage suppressor (TVS) to protect from transient overvoltage conditions originating in either the converter or the load circuitry. The power system designer must insure against "nuisance tripping" of the overvoltage detector in the converter. Both trimming the output voltage of the converter upwards and the usage of remote sensing will increase the voltage level at the converter and reduce the margin between the DC output voltage setting and the overvoltage trip point. This will decrease the available room for voltage transients due to load dynamic switching activity.

Overtemperature detection and shutdown is a valuable feature for systems using forced air cooling due to the number of failure modes and relatively high failure rates of the cooling hardware. System temperatures can rise due to a fan failure, dirty air filters or a loss of airflow for other reasons. The more difficult question is where to locate the temperature sensors - internal to the converters or externally in the system. In general, using overtemperature sensors internal to the power converters makes more sense for centralized systems where there are fewer converters operating at higher power levels. In card-level DPA systems, including overtemperature detection internal to every converter is usually not needed due the number of converters and their dependence on a common airflow path. In this situation, one or two system-level temperature sensors can be used to advantage. Some converters will have a "thermal warning" diagnostic output that is issued before the converter actually shuts down. This can be useful in some situations, but unless there are service personnel on site to remedy the cooling situation immediately, the system will soon shut down anyhow. In most situations,

it makes more sense to use at least one "thermal warning" sensor in the system rather than imbedding it internal to a power converter. When doing diagnostics using converters with internal overtemperature detectors be aware that the converters can have significant thermal mass and that the overtemperature sensors are usually designed with hysteresis so that they will not power up until the temperature drops below the turn-off level. Consequently, the converters will need perhaps several minutes to cool down before it can be determined if they will successfully power up again.

Some converters will issue a "power good" signal that indicates that its output is within regulation limits. This is most useful in a system with only one converter so that the converter's output signal can be used as an indicator of the total powersystem's health. But most systems have several converters, and the power good output of all the converters would need to be "anded" in order to arrive at an overall assessment of the power system status. In practice, it takes very little more in the way of ICs and wiring to sense each voltage at the load and generate an overall power good status signal for the complete assembly or system. This will be a more flexible approach and is recommended for most systems that utilize multiple converters. The power good signal internal to the converter is most often used for centralized converters with multiple outputs and on Front-End converters in DPA systems.

A current monitor is a circuit internal to a converter that senses its output current and issues a voltage proportional to it. It is most useful for high current converters in centralized systems with the capability of adding or subtracting load function. In this type of scenario, the current monitor will give an indication of the

total system load at any point in time. The most common example is the Front-End converter for DPA systems, where many of the available converters contain such a function. A current monitor will be much less useful in shelf-level and card-level DC/DC converters.

The relative usefulness of converter diagnostic features is summarized in the following table:

Feature	Centralized	Shelf-level	Card-level
Overcurrent	High	High	High
Overvoltage	High	High	Medium
Overtemperature	Medium	Medium	Low
Power Good	High	Medium	Low
Current Monitor	Medium	Low	Low

Table 3 - Relative Importance of Converter Diagnostics

As an example of how diagnostics could be handled in a typical DPA system, we will consider a card-level system and look at how the card failure isolation and replacement could be done in the event of a fault. The diagnostics for shelf-level and centralized systems will be more complex in nature and beyond the scope of this brief treatment. It is assumed that the Front-End AC/DC converter will have panel mounted LEDs or indicators to allow assessment of its condition, and that the fault is isolated in nature such that only one load card is non-functional. In some systems, the functional diagnostics associated with the circuitry itself could be sufficient to point to the failed card. In that case, the card could be replaced without even the need for determining whether the fault was related to the on-card converters or to the load circuits. For this example, we will assume that this level of functional diagnostics does not exist and that it is desired to isolate the faulty card by monitoring of the on-card power converters.

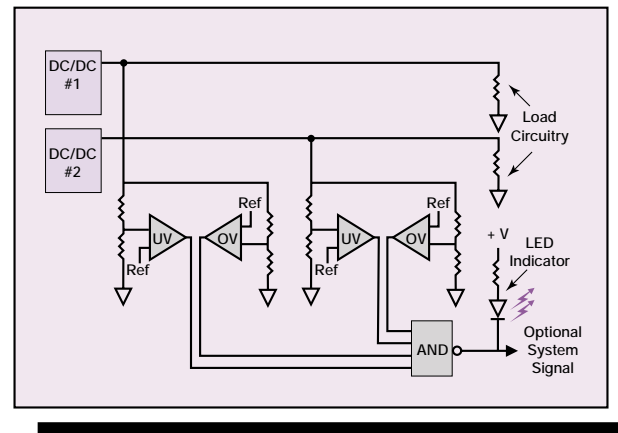


Figure 5.36 - Typical Card-Level Voltage Monitoring Circuitry

One common, simple and yet effective approach for the on-card diagnostic circuitry is shown in Figure 5.36. Each DC voltage is monitored for both undervoltage and overvoltage by means of comparator circuitry. This can be done inexpensively with either conventional discrete IC circuitry or with some of the newer power supply supervisory circuits. If the converters contain overvoltage shutdown circuits, then the system-level overvoltage comparators can most often be eliminated. Two converters are shown for simplicity, but any number can be monitored in a similar way. The comparator outputs are then anded to obtain an overall "power good" signal for the entire card which is used to drive a LED on the card and perhaps a signal to the higher-level system diagnostics processor. Since we are looking for a power fault, and using a non-active indicator to signify a fault, it is OK to power these detector and indicator circuits with one of the on-card converter output voltages. We will assume for now that it only lights the LED and that manual diagnostics is required to isolate the faulty card. As we saw earlier, all of the expected fault types, other than possibly an overtemperature fault, will result in either an overvoltage or undervoltage condition and will be detected by this approach. A

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system-level overtemperature detector can easily be added to this circuit.

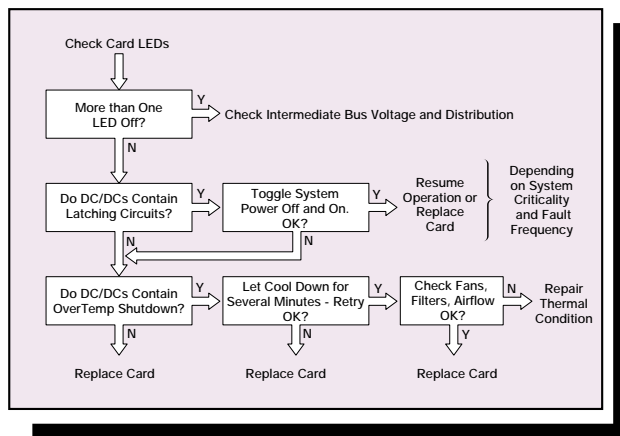


Figure 5.37 - Diagnostics Flow Chart for Card-Level DPA System

It is assumed that the repair strategy is to replace the card containing the fault with a new one and then perhaps repair the faulty card later at a separate facility. The isolation of a power fault to the card level then consists of basically looking for cards without an active LED. A more regimented overall approach is shown in the flowchart in Figure 5.37. Using the procedure shown here, the diagnostic circuitry will also help with the isolation of the following conditions:

- Problem with intermediate bus voltage
- Transient failures
- Cooling and thermal issues

Note that if the on-card converters contain latching type fault circuits for overvoltage or overcurrent, it is recommended to first toggle the input power source to see if the fault can be reset to a normal condition. Similarly, overtemperature shutdown circuitry can be re-tried, but only after sufficient time has elapsed for the

converter to cool down to a normal operating temperature. This example illustrates the relative ease of accomplishing diagnostics in a card-level DPA system.

5.5 Paralleling of Power Converters

Paralleling power converters is done for one of two reasons - increasing power output capability or providing redundancy. Figure 5.38a shows an example of paralleling two DC/DC converters to increase the power output. The effect of redundancy on system availability will be developed in Chapter 8 so we will only discuss the actual interconnection mechanisms in this section. We will discover that, with card-level DPA systems, redundancy can be achieved without the need for actually paralleling DC/DC converters. This is fortunate, because directly paralleling DC/DC converters for the purposes of redundancy adds complexity and reduces the overall conversion efficiency of the power system. The most common successful application of partitioning for redundancy is the Front-End converter system for DPA systems. To provide immunity from the loss of one Front-End converter, several are configured in a "n+1" arrangement as shown in Figure 5.38b. Should one converter fail it will isolate itself from the intermediate bus and the other converters will supply the entire load current.

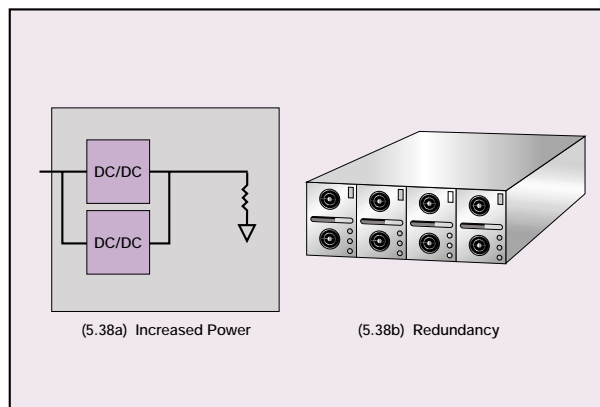


Figure 5.38 - Types of Paralleling

Current Sharing - When two or more power converters are paralleled, an important consideration is the amount of current that each one supplies. In some implementations they can supply vastly different amounts of current. In other designs, they can provide approximately the same amount of current, referred to as "current sharing". Current sharing can be desirable in many circumstances but is not essential in some applications.

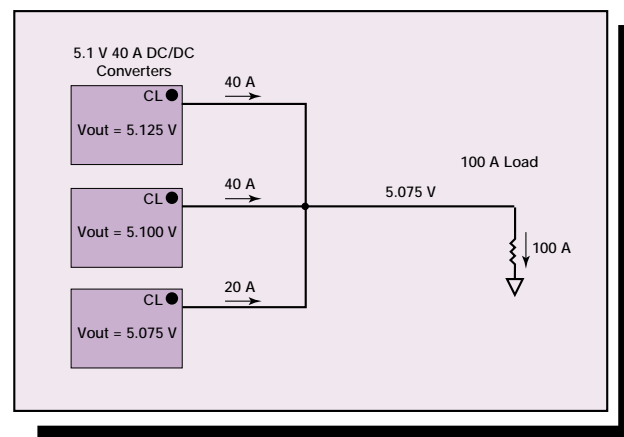


Figure 5.39 - Paralleling without Current Sharing

For purposes of explanation, consider the paralleled DC/DC converter system shown in Figure 5.39. In this example there are three 40A converters operated in parallel to supply a 100A load. Each converter has a nominal output voltage set point of 5.1V, but each one has some variation around the nominal, ranging from 5.075V to 5.125V. For purposes of illustration, we will assume that the output impedance of the converters is zero and that there is no resistance in the system power distribution. In this configuration, the converter with the highest output voltage (the upper one in this example) will supply all of the current until it reaches its overcurrent limit of 40A. At this point, its output voltage starts to drop (continuous current limiting is assumed) until it

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reaches 5.1V, at which point the second converter starts to supply current. The second converter will also reach its current limit, and its output voltage will drop down to 5.075V, where the third converter will begin to supply current. In the steady-state condition, all three converters will supply current - 40A each for the top two and 20A for the bottom one. The system output voltage will be equal to 5.075V. The top two converters will be operating in current limit with constant current output, while the bottom one will be operating below current limit in constant voltage mode.

There is nothing inherently wrong with this arrangement, which is referred to as **direct paralleling without current sharing**. If the converters' overcurrent implementation is such that they switch to a continuous current mode without degradation in failure rate, this system will be operable. The Artesyn SXA10 DC/DC converters, for example, are designed to be directly paralleled without degradation in reliability. This approach should, however, be used with caution. With latching or fold-back type overcurrent circuits, this system will either not work or be subject to intermittent faults! Also be aware that many converters dissipate extra power when operated in current limit and this increases their failure rate. For these reasons, direct paralleling without current sharing should only be used if specifically recommended by the converter manufacturer.

In practice, there will be some distribution resistance that will result in more equal current sharing than indicated in Figure 5.39, but one or more of the converters could still be operating in current limit mode. **Passive current sharing** is a technique for using the resistance of the distribution system to control the balance between the converter currents and prevent any of them from

operating in overcurrent mode. As a minimum, the resistance inherent in the distribution system will need to be analyzed to determine its effect on current sharing. In other cases, extra resistance will need to be added in order to satisfy the current sharing objectives.

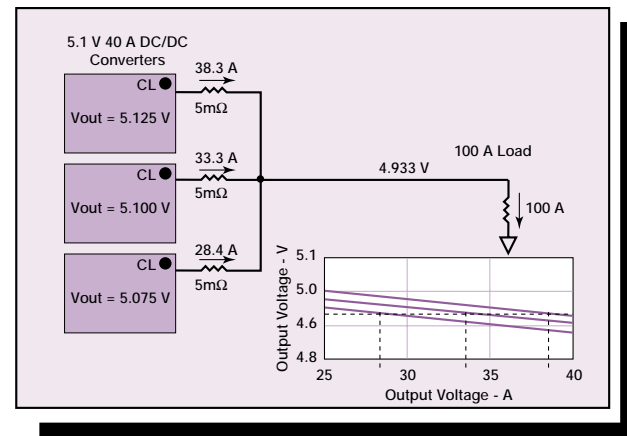


Figure 5.40 - Passive Current Sharing

A passive current sharing setup is shown in Figure 5.40, using the same converters as in the first example. The only change has been to add 5mΩ of resistance in each leg of the distribution system. The load output voltage vs. current characteristic of each of the three converters is shown in the graph. Note the resistive regulation slope that has resulted. The system will reach a steady-state condition with an output voltage of 4.933V due to the resistive drops. The currents out of each converter will range from 28.4A to 38.3A, a much closer balance than the previous example without resistance. Now, none of the converters are operating in current limit, allowing the usage of converters with a wider range of current limit implementations. Increasing the resistance value will improve the current balance, but at the expense of additional voltage drop at the load and decreased distribution efficiency. This is the major design trade-off involved with passive current sharing. The voltage at the

load can be raised, if desired, by trimming the output voltage of each of the converters upward.

It is possible to improve the current sharing performance of paralleled converters by adjusting the output voltage of each converter to a common value by using the resistive voltage trim capability. This technique is referred to as "**selective trimming**". The downside of selective trimming is that it requires extensive manual measurement and adjustment. This is often acceptable in a low-quantity production environment or for prototype systems, but creates significant problems in high volume manufacturing or for field service situations. If a new converter is installed, there will, in general, need to be a unique resistor value installed with it. Selective trimming is therefore not often used as a solution to the current sharing problem in high volume systems.

The voltage vs. current characteristic shown in Figure 5.40 can be designed into a converter rather than relying upon external resistance in the distribution system. Synthesizing the characteristic into the feedback circuit so that the output regulation is not "stiff" like an ideal voltage source, but rather "soft" results in a converter with essentially higher output impedance. This approach does not incur the efficiency loss penalty of passive current sharing, and is referred to as "**slope**" or "**droop**" current sharing. It can be useful in situations where tight voltage regulation is not required - most often in low power systems. One advantage of this approach over passive current sharing is that the current sharing is designed into the converter rather than requiring any system-level analysis.

Active current sharing is a technique for achieving current balance without the disadvantages of additional

power losses or reduced voltage regulation. In return for these advantages, the converters must be interconnected with a separate current sharing signal, which allows for communication between them. Some converters are designed to operate in a "**master / slave current sharing**" configuration. In this case, one converter assumes control of the others and sets the output voltage as shown in Figure 5.41a. The current balance using this technique is typically within 10%. Note that if paralleling for redundancy is attempted with this design, and the master converter fails, the system will fail.

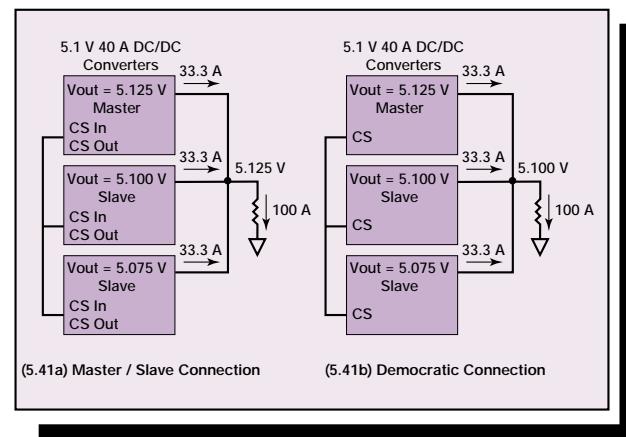


Figure 5.41 - Active Current Sharing

A more robust active current sharing technique is called "**democratic current sharing**", and is illustrated in Figure 5.41b. As the name implies, there is no designated master converter. All interconnected converters are treated equally and participate together to set the output voltage and determine the current balance, again to within 10% or so. An example of this approach is the Artesyn NXI110 VRM module. This design allows several additional modules to be connected, and each of the output currents will automatically be configured to be equal to the total current divided by the number of interconnected modules. As a consequence, modules

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can be added to or removed from the system to accommodate load changes or desired operating current levels without the need for any system redesign.

Paralleling for Redundancy - Redundant elements are sometimes used in high availability systems so that the system can remain operational in the event of a failure of any one element. This is commonly done in the Front-End off-line converters of a DPA system, the Artesyn AFE series for example. If the concept is extended to the DC/DC converters, however, it is not usually as successful. We show such a connection in Figure 5.42. Here we connect two DC/DC converters in parallel, each of them capable of supplying the entire load power, so that the load will remain operational in the event of a single converter failure. To address the possible fault modes we need to add several circuit elements in addition to a directly paralleled connection. Each output must be isolated by a forward biased diode. In the event that a converter fails with a shorted or low impedance output, this will prevent it from dragging down the load voltage. These diodes will present problems in low voltage circuits or for systems with high efficiency requirements. With a 2.5V load, for example, the 0.5V diode voltage drop will turn an 85% efficient converter into a 73% efficient converter!

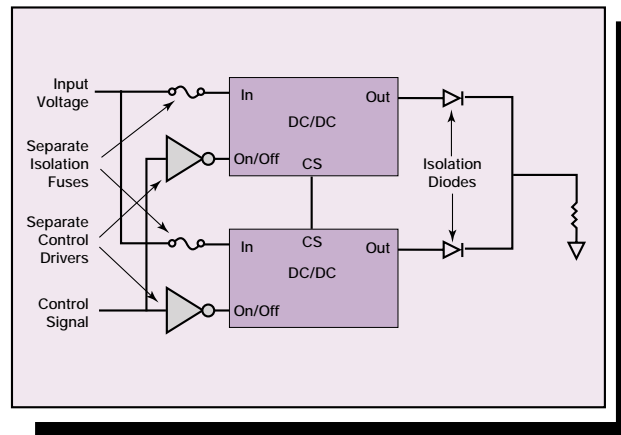


Figure 5.42 - Paralleling for Redundancy

There is a possibility that the input of the converter could fail in a shorted condition. To prevent this from disabling the other converter, both converters must be individually fused close to their inputs. Separate control drivers should also be used so that a fault on the remote on/off input will not affect the other converter(s). As can be seen from the figure, this type of configuration can rapidly get fairly complex, especially if other control/diagnostic functions or remote sensing is used. Even with this elaborate connection, there are still several common failure modes that are not protected against - the input source voltage, the control signal, load distribution, etc. The latest generation DC/DC converters are extremely reliable - in the same ballpark as the load circuitry - so it does not usually make sense to attempt an arrangement like this. A better approach with card-level partitioning is to make the entire card function redundant. Then each circuit and its associated non-redundant power converter(s) can be replaced as a unit if there is a fault in either the load or the power.

Additional Considerations - Before making a decision to use paralleled converters, there are some additional

considerations to keep in mind. For most systems cost and reliability are both important factors. If two 40W converters are paralleled, for example, they will have approximately twice the total number of internal components as one 80W converter. As a consequence, both total cost and the total failure rate will increase. Therefore if a single converter is available that will handle the load current, it is usually a better choice than paralleling two or more smaller ones.

Many of the latest DC/DC converters intended for low voltage applications use synchronous rectification to achieve high efficiency. Depending upon the converter topology, these converters can be damaged by directly paralleling them. Using isolation diodes will sometimes alleviate this problem, but at the expense of significantly degraded efficiency. It is recommended to be especially careful about paralleling synchronous rectifier converters - in fact, only do so if specifically allowed by the manufacturer.

Recommendations - We have seen that paralleling is a viable approach for increasing the output power or availability of power converters. But we have also discussed its limitations and disadvantages. In general, paralleling is something that is best avoided unless there is no other solution. The two most common ways of avoiding the need for paralleling DC/DC converters are:

- Select a single converter with a higher power rating
- Re-partition the load so that lower power single converters may be used

The above solutions are easier now than ever before because of the much greater availability of converters

with wide ranges of power and output voltage.

The following types of converter systems were specifically designed with paralleling in mind and the reader is encouraged to utilize the advantages of both modular power capability and availability:

- N+1 AC/DC converters for DPA front ends
- Modular democratic current sharing VRM systems.